FEDERAL UNIVERSITY OF PAMPA

Tailize Cordeiro de Oliveira

A Closed-Loop Regulated Voltage UHF RF Energy Harvesting System for Ultra-Low Voltage Applications

Alegrete
May, 2024

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Dissertation presented to the Graduate Program in Electrical Engineering of Federal University of Pampa, as a partial requirements for the obtaining the Master's Degree in Electrical Engineering.

Supervisor: Prof. Dr. Lucas Compassi Severo
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TAILIZE CORDEIRO DE OLIVEIRA

A CLOSED-LOOP REGULATED VOLTAGE UHF RF ENERGY HARVESTING SYSTEM FOR ULTRA-LOW VOLTAGE APPLICATIONS

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I dedicate this work to my father Cláudio, my brothers Anderson and Antônio, and my boyfriend Marcelo for their support and affection during difficult times.

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ABSTRACT

Harvesting the energy available in the environment is a promising strategy for powering ultra-low voltage (ULV) devices and replacing the batteries. Replacing the batteries in these devices is a complex task, making it necessary to use alternative energy sources. Among the energy sources available in the environment, RF signals stand out because they have a lower power density range and are suitable for powering ultra-low power devices. However, the RF power that is collected by the receiving antenna is not constant, and as the electronic devices need a constant supply voltage, a system capable of collecting the RF signal and converting it into a stable and regulated DC output voltage is demanded. Thus, in this dissertation, a complete RF energy harvesting (RF-EH) system that provides a stable DC supply voltage of 0.4 V is proposed to power devices in ultra-low power and ultra-low voltage applications. A closed-loop self-starting impedance tuning system, based on shunt transistors, is proposed and adopted to automatically regulate the DC output voltage of the RF-EH system. The proposed system is implemented at the schematic and layout levels in a 65 nm low-voltage CMOS process. The power conversion efficiency (PCE) of the closed-loop RF-EH, considering the post-layout result, is 50% at an input power level of -15 dBm, and frequency of 915 MHz, when generating 0.4 V of output voltage for a 10 kΩ load. The proposed solution is implemented on a chip with an effective area of 0.045 μm^2 and demonstrated to power ultra-low voltage batteryless devices with a regulated output voltage of 0.4 V and output power levels of dozens μW range.

Keywords: Energy harvesting, radio frequency, CMOS process, batteryless.

RESUMO

A coleta da energia presente no meio ambiente é uma estratégia promissora para alimentar dispositivos de ultra-baixa tensão (ULV) e substituir o uso de baterias. A substituição das baterias destes dispositivos é uma tarefa complexa, tornando necessária a utilização de fontes de energia alternativas. Dentre as fontes de energia disponíveis no ambiente, os sinais de RF destacam-se por possuirem uma grande disponibilidade com um escala de densidade de potência mais baixa, sendo adequados para alimentar dispositivos de potência ultra-baixa. No entando, a potência de RF que é coletada pela antena receptora não é constante, e como os dispositivos eletrônicos necessitam de uma tensão de alimentação constante, tais sistemas necessitam possuir a capacidade de coletar o sinal de RF e converter para uma tensão de saída DC estável e regulada. Assim, nesta dissertação, é apresentado um sistema completo de coleta de energia baseado em sinais de RF que fornece uma tensão de alimentação DC estável de 0.4 V para alimentar dispositivos de aplicações em ultra-baixa potência e ultra-baixa tensão. Um sistema de sintonização de impedância auto-inicializado em circuito fechado, baseado em transistores-shunt, é proposto e adotado para regular automaticamente a tensão de saída DC do sistema RF-EH. O sistema proposto é implementado à nivel de esquemático e layout num processo CMOS de 65 nm. A eficiência de conversão de energia (PCE) do RF-EH de circuito fechado, considerando resultado pós-layout, é de 50% a um baixo nível de potência de entrada de -15 dBm e uma frequência de 915 MHz, que gera 0.4 V de tensão de saída para uma carga de 10 kΩ. A solução proposta é implementada num chip com uma área efetiva de 0.045 μm^2 e demostra capacidade para alimentar dispositivos de ultra-baixa tensão sem bateria com uma tensão de saída regulada de 0.4 V e potência na faixa de dezenas de μW.

Palavras-chave: Coleta de energia, radiofrequência, processo CMOS, sem bateria.

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1 INTRODUCTION

The evolution of technology and the need for increasingly compact, versatile and efficient portable devices implies a great advance in microelectronics. For decades, power consumption has been one of the most discussed debates, and in the complementary metal oxide semiconductor (CMOS) process, the miniaturization trend is increasingly focusing on low-voltage, economic processes and high performance to meet the requirements of cutting-edge mobile devices (RADAMSON et al., 2020).

However, when it comes to energy sources for these devices, there is still a long way to go in terms of technological evolution. As Muhammad et al. (2022) points out, electricity plays a fundamental role in carrying out most of our society's daily activities, where current technological progress recognizes energy as one of the main challenges, given the possibility of shortage.

Also, according to Andrae e Edler (2015) from Huawei Technologies Sweden AB, the global electricity consumption attributed to communication technology (CT) by 2030 may exploit more than 51% of global electricity consumption. And to circumvent this, other sources of sustainable energy need to be explored.

To meet the need for energy sources in electronic devices, the main device currently used is batteries, and according to Chun, Ramiah e Mekhilef (2022), their constant use has numerous drawbacks, such as environmental pollution (highly flammable equipment), short lifespan, high replacement costs and maintenance restrictions.

To get around this, it would be better to use a system that is capable of harvesting energy from alternating sources and transmitting it wirelessly and without storage. Thus, integrating an alternative energy collection system into a single device would allow greater autonomy and independence for typical applications, such as biomedical implants and space applications, for example. The development of new, more sustainable and practical energy supply techniques is emerging as a necessity.

Recent studies have considered the Energy Harvesting (EH) technique to reduce and, in some cases, even replace the use of batteries (DE-OLIVEIRA et al., 2023). Thus, EH is basically defined as the ability to harvest available energy from the external environment from known sources such as solar, thermal, vibrational and radio frequency (RF) (MIL et al., 2010; TRAN; CHA; PARK, 2017). This technique is already known and has been widely used to reduce environmental impacts.

Table 1 shows the properties of various renewable energy sources, including their characteristics, efficiency and power density. In the case of radio frequency (RF) energy, we find that it has a minimum power density ranging from 0.001 to 0.1 $\mu W/cm^2$. This range is capable of meeting the power demand of small electronic devices such as electronic watches, calculators, RFID tags and hearing aids (MUHAMMAD et al., 2022).

In addition, according to Muhammad et al. (2022), the power density of ambient RF signals is increasing due to the development of mobile phone networks, entertainment

based on television (streamers) and Wi-Fi applications. This means that the RF signal is becoming more available compared to other power sources, due to its ubiquity and ability to reach environments in which other sources are not present. This makes it an excellent alternative, including in extreme locations such as biomedical implants, aerospace applications, for example. Moreover, due to its smaller scale of power density, it is perfectly suited to supply ultra-low power devices.

Table 1 – Power densities of typical energy harvesters.

Energy source	Characteristics	Efficiency	Power density
Light	Outdoor	10 - 25%	100 mW/cm^2
	Indoor		100 μW/cm^2
Thermal	Human	0.1%	60 μW/cm^2
	Industrial	3%	10 mW/cm^2
Vibration	Hz-Human	25% - 50%	4 μW/cm^2
	kHz-Machines		800 μW/cm^2
Radio frequency	GSM 900 MHz	50%	0.1 μW/cm^2
	WiFi 2.4 GHz		0.001 μW/cm^2

Source: (MIL et al., 2010).

1.1 WIRELESS COMMUNICATIONS AND RF ENERGY HARVESTING

The advancement of society further drives the advancement of wireless communication, as this technology allows instant access to information from anywhere in the world without the need for physical cables. Advanced smartphones, implantable medical devices, wireless sensor networks, industrial automation, internet of things, 5G and 6G technologies are examples that demonstrate this continuous progress.

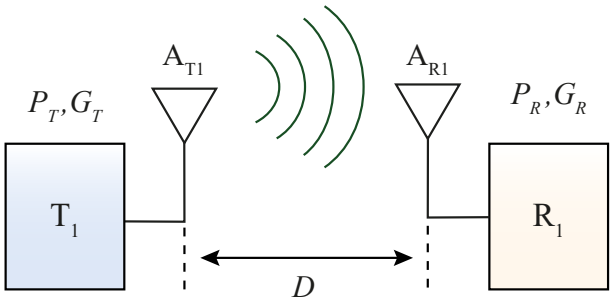
In addition, there are several forms of wireless communication, such as Wi-Fi, Bluetooth, RFID, mobile devices and communication satellites.

In this context, the study of RF-EH becomes even more essential. This technology is capable of picking up signals over longer distances compared to other wireless charging systems, such as magnetic resonance and magnetic coupling methods (CHUN; RAMIAH; MEKHILEF, 2022).

A typical RF-EH system consists of an antenna that receives and collects RF energy and then an RF-DC converter. Thus, in order to implement the RF-EH technique, initial concepts of RF signal propagation must be understood.

From Figure 1 we can exemplify the principle of RF signal transmission, where there is an antenna that transmits the signals and another that receives these signals. The distance between these antennas is defined as the RF transmission distance, and from this concept, there are two characteristics defined by Fraunhofer, namely, near field and far field (BALANIS, 1992).

Figure 1 – RF transmission principle. T_1 is transmitter 1, R_1 is receiver 1, A_{T1} is the antenna transmitter 1, A_{R1} is the antenna receiver 1, D is the RF transmission distance, P_T is the transmitted power , P_R is the received power, G_T is the gain of the transmit antenna, and G_R is the gain of the receiver antenna.



The classification of an RF-EH whether it is near field or far field, is given from the power density, operating frequency and transmission range of the RF energy that is being harvested (CHURCHILL et al., 2020).

In an RF-EH the transmitter and receiver antenna are close in distance $(2d^2)/\lambda$, where d is defined as the diameter of the antenna and λ the wavelength of the RF signal. Thus, when the transmission range of the propagated RF signal is beyond the Far-Field distance, the system is classified as dedicated far-field or ambient RF-EH, and the far-field E (electric field) and H (magnetic field) fields have equal magnitudes at different points in space (CHURCHILL et al., 2020).

Also, according to Muhammad et al. (2022) the exponential growth of wireless technology draws attention to RF-EH from ambient electromagnetic waves radiating in space. Therefore, in this work we adopt the RF-EH Far-Field system and the received power can be predicted through the Friis transmission equation 1.1 (FRIIS, 1946):

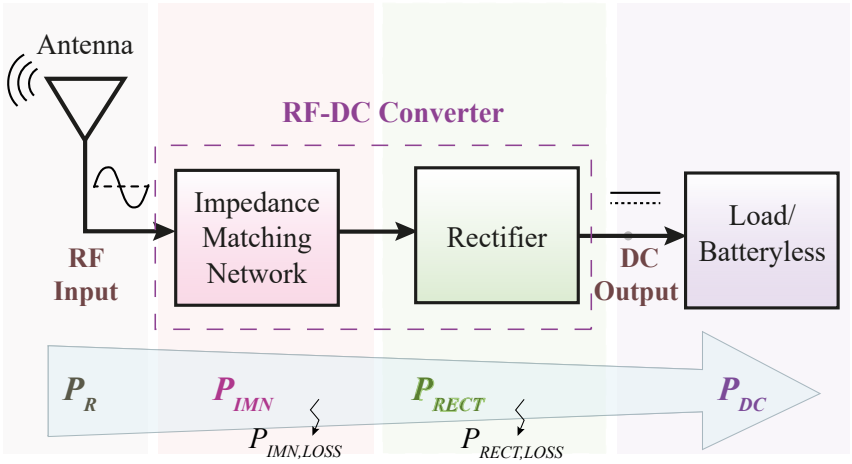
$$P_R = \frac{P_T G_T G_R \lambda^2}{(4\pi D f)^2} \tag{1.1}$$

Here, P_R is the received power, P_T is the transmitted power, G_R is the gain of the receiving antenna, G_T is the gain of the transmitting antenna, λ is the wavelength, D is the distance between the transmitting antenna and the receiving antenna and, f is the frequency of the RF wave. Therefore, the received power density varies dynamically with the transmission distance. However, it must be considered that there are several RF bands, as shown in Table 2, and the strength of the signals of each one depends on the medium where they are located.

Studies carried out by Piñuela, Mitcheson e Lucyszyn (2013) and Chun, Ramiah e Mekhilef (2022), show that the ultra-high frequency (UHF) bands GSM900 and GSM1800 were the ones that showed the highest measured power density in urban environments.

However, the other bands can also be used in the RF-EH design, and according to Chun, Ramiah e Mekhilef (2022) the choice of the appropriate frequency to be collected depends on the individual specifications of each application, and also on the location.

Figure 2 – Typical RF-EH and input-output powers.



In this sense, the choice should be based on the availability and reliability of the power density of the site to be explored.

Due to the higher power attenuation from the transmitter to the received path, the efficiency of the RF to DC conversion should also be evaluated. The ratio between the power received by the antenna and the output power delivered to the load in an EH-RF system is the power conversion efficiency (PCE), given as:

$$PCE = \frac{P_{DC}}{P_R} = \frac{V_{OUT} I_{OUT}}{RMS(V_{IN} I_{IN})} \cdot 100 \tag{1.2}$$

As illustrated in figure 2, the power consumed by the impedance matching network (P_{IMN}) and by the rectifier (P_{RECT}) is lost and need to be minimized to a better PCE.

Table 2 – Frequency bands and ranges.

Frequency Band	Frequency Range (MHz)
VHF	30 - 300
FM	87.5 - 108
UHF	300 - 3000
TV	470 - 862
GSM900 UL	890 - 915
GSM900 DL	935 - 960
GSM1800 UL	1710 - 1785
GSM1800 DL	1805 - 1880
UMTS UL	1920 - 1980
UMTS DL	2110 - 2170
LTE UL	791 - 821, 880 - 915, 1710 - 1785, 1920- 1980, 2500 - 2570
LTE DL	832 - 862, 925 - 960, 1805 - 1880, 2110 - 2170, 2620 - 2690
Wi-Fi	2400 - 5000 - 6000
ISM	433, 915, 2450, 5800

Adapted from (CANSIZ; ALTINEL; KURT, 2019).

1.2 ULTRA-LOW VOLTAGE APPLICATIONS

The exponential advance of technology, where electronic devices are moving towards miniaturization in order to reach more people, such as implantable biomedical devices, portable devices and the Internet of Things (IoT), means that there is a need for power sources that are also miniaturized and have high precision. In addition, the main challenge facing today's electronic devices is energy saving and energy efficiency.

Thus, ultra-low voltage and ultra-low power devices have been explored as an attractive and crucial alternative to meet the need for batteryless electronic devices, where reducing energy consumption and minimizing heat dissipation is fundamental.

Ultra-low power refers to devices that consume minimal energy, extending battery life and enabling the use of alternative energy sources, such as energy harvesting. Additionally, ultra-low power operation allows for the implementation of "deep sleep" and energy-saving modes, where parts of the circuit are powered down when not in use.

Thus, a major challenge in designing RF energy harvesting (RF-EH) systems using the CMOS process for ultra-low power applications is to minimize the silicon area occuped, thereby making the design more economically efficient, while ensuring optimal power conversion efficiency (PCE). To achieve this, using an ultra-low voltage of 0.4 V becomes a viable option. When designing a rectifier to convert RF to DC, if the desired output voltage is very low, fewer rectification stages are needed, simplifying the design. This allows the circuit to be a single-stage design, where its efficiency is maximized when the output voltage reaches 0.4 V.

1.3 OBJECTIVES

The main objective of this work is to design an integrated RF-EH system able to provide a regulated voltage of 0.4 V to be used as a supply voltage in ultra-low power batteryless devices from an RF frequency collected in the 915 MHz UHF band.

The RF-EH system must be self-regulated, maintain a constant output voltage, and provide its own supply voltage. It should also reach the maximum peak PCE at the lowest input power level, in order to be suitable for batteryless applications. Furthermore, the system should be engineered to control the output voltage by considering a range of RF signal amplitude values and load conditions. Lastly, this design seeks to make a meaningful contribution to research in the area of RF microelectronics.

1.4 DISSERTATION ORGANIZATION

This work is divided into 5 chapters. Chapter 1 deals with the introduction to RF-EH, containing the main gaps and challenges, the motivation for this work and a brief introduction to communication via RF signals.

Chapter 2 covers the literature review on RF-EH, containing the main RF-DC conversion blocks (Rectifier and Impedance Matching Network).

Chapter 3 contains the design flow for RF Energy Harvesting.

Chapter 4 includes the design of the RF-EH from three versions, as well as a comparison of the best performance.

Chapter 5 contains the complete design of all the RF-EH blocks, as well as individual and complete system layouts with post-layout results, and the prototyping of the IC.

Finally, Chapter 6 contains the conclusion of this dissertation, with the main contributions addressed, proposed future work and publications obtained during the research.

2 RF ENERGY HARVESTING

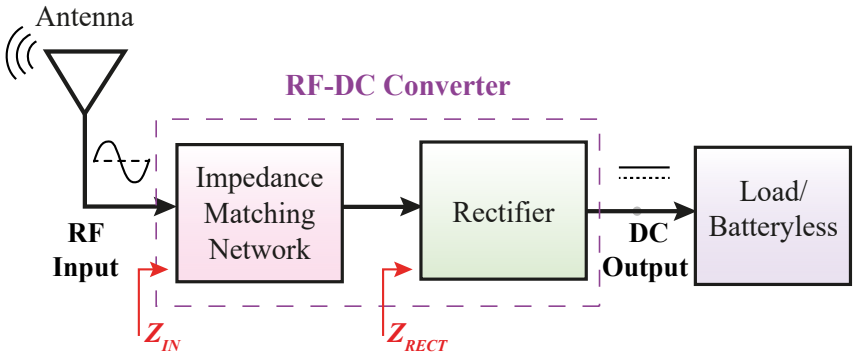
In a RF-EH system, the energy received may or may not be sufficient to power an electronic device (TRAN; CHA; PARK, 2017). If the power collected and converted by the RF-EH is lower than the value required by the device, it needs to be accumulated to the minimum value so that the device can operate for some time. However, there is a recent trend towards the use of batteryless devices (SABOVIC et al., 2020). Batteryless is being implemented as a more sustainable vision, based on reducing the use of batteries in electronic devices.

Thus, in order to be able to power an electronic device, that is, a load, from the extraction of energy from electromagnetic waves, it is necessary to design an RF-DC converter. In this chapter, a general theory about the RF-DC converter will be presented, containing its main blocks: the Rectifier and the Impedance Matching Network. A literature review about the types and the main and most recent circuits used in both topologies will also be presented. In addition, a literature review of the techniques used in RF-EH is presented to contemplate specific applications.

2.1 RF-DC CONVERTER

The main source of energy for electronic devices is DC voltage, so to use the RF energy harvesting (RF-EH) technique for this purpose, it is necessary to design a front-end system capable of capturing RF signals and converting it into DC voltage. The system that can perform this operation is called RF-DC converter, as shown in Figure 3.

Figure 3 – RF-to-DC conversion principle.



Therefore, in Fig. 3 we can observe that the first stage of the RF-EH system is the capture of the RF signal by means of a receiving antenna, the electrical model of this antenna is represented through an AC source with amplitude V_{AMP}, set at the frequency of interest and a characteristic impedance Z_0. Thus, the characteristic of the collected RF signal is a sine waveform.

In sequence, the main block of this front-end is the rectifier. Rectifiers are based on using the diode semiconductor device for AC-DC conversion. However, when dealing

with RF, its variable nature and propagation losses at high frequency must be considered (LIAN et al., 2023). That is, if the input impedance of the rectifier Z_{RECT} (considering the load in parallel) is different from the impedance Z_0 of the antenna, a portion of received power is reflected, causing impacts on the antenna performance and also on the RF-EH.

According to Lian et al. (2023) there must be a trade-off between power conversion efficiency (PCE) and the sensitivity of the energy harvesting device. This makes it more challenging to design a rectifier for RF-EH. Therefore, it can be seen from Fig. 3 that before rectification we must design an impedance matching, which will ensure maximum transfer of signal power to the final load.

Thus, in this section, the basic topologies of rectifiers, based on diodes, which are fundamental for the understanding of the rectification principle, as well as the fundamentals of impedance matching design, will be addressed. In addition, the CMOS transistor-based rectifier topologies and a bibliographic review of the latest works in the literature will also be presented, as well as works that contemplate the impedance matching techniques adopted in RF-EH systems.

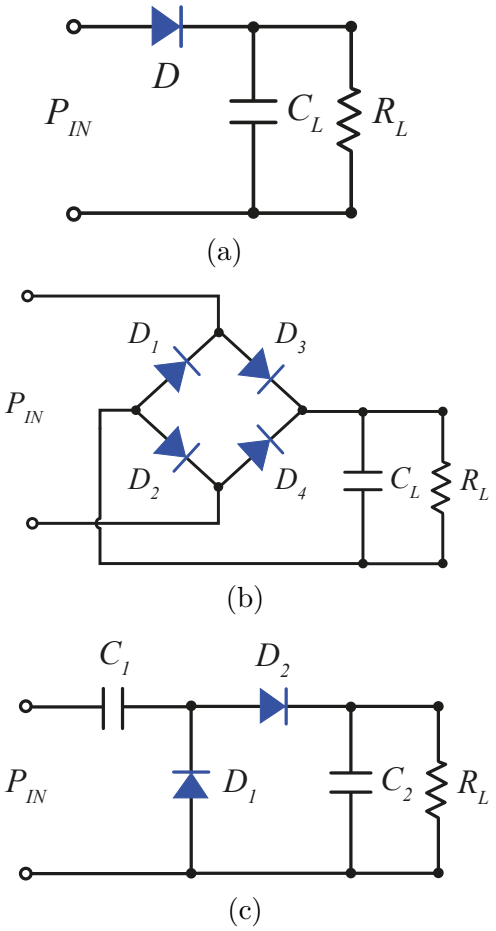
2.1.1 RECTIFIER

The rectifiers can be represented by the three basic topologies shown in Figure 4: half-wave, full-wave bridge, and charge-pump.

The half-wave rectifier shown in Figure 4a is the simplest configuration. It has only one diode and its working principle basically consists of two phases, where in the first phase the input current flows in the positive direction from the source, turning the diode forward biased. In this condition, the current flows to the load (R_L). During the positive half cycle, the amplitude of the output voltage signal is similar to that of the input amplitude. In the second phase, the input current flows in the negative direction, resulting in a reverse bias. In this phase, the output voltage has the same input signal amplitude. The main characteristic of this rectifier is its simplicity. However, it is unsuitable for common applications, because by allowing the passage of only one of the semi-cycles, the output voltage is discontinuous and the power of the AC voltage seen in the voltage output is always half, reducing the maximum conversion efficiency.

In order to make the circuit work in both AC cycles, the use of topologies with more diodes is an option. A topology that contemplates this solution is called a bridge full-wave rectifier, as illustrated in Figure 4b. This topology allows the signal seen at the rectifier output to be continuous, i.e. when the input sine wave is positive, diodes D_3 and D_2 conduct, while D_1 and D_4 are blocked. When the wave is operating in the negative cycle, diodes D_1 and D_4 are conducting, while D_3 and D_2 are blocked. However, a disadvantage of this topology is the voltage drop across diodes, since there are always two diodes in conduction in the current path, which causes a higher power and voltage loss.

Figure 4 – Basic rectifier topologies: a) Half-wave; b) Full-wave bridge; c) Charge-Pump/Doubler.

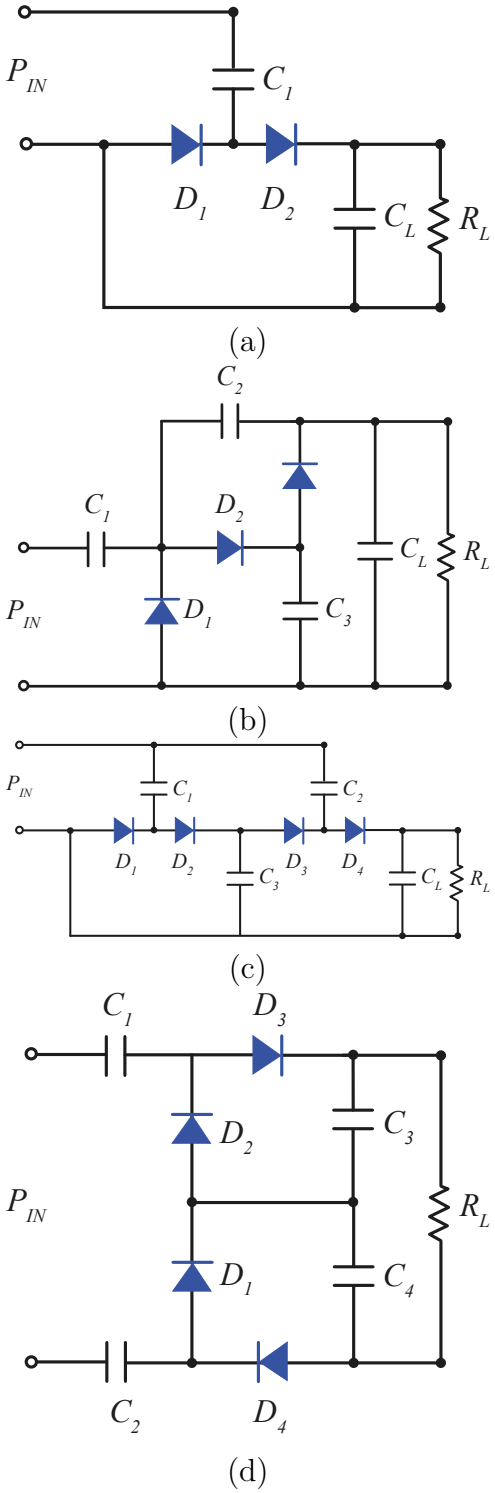


A third rectifier solution is the so-called doubler or charge pump. This topology, as illustrated in Figure 4(c), transfers the input signal to the output in the same way as the full-wave rectifier, but capacitors are included in its circuit, which stores the voltage as the diodes are driven, eventually transferring to the output twice the value of the input peak voltage. According to Tran, Cha e Park (2017), this topology has better efficiency when compared to the half-wave and full-wave topologies.

Other configurations, based on the three basic rectifier configurations, but more suitable for RF applications, are represented in Figure 5. The differences between them are related to the levels of derivation to reduce parasitic effects and the resulting power conversion efficiency.

The construction of the Dickson-Greinacher and Greinacher is based on Charge Pump topology. The Dickson variations are based on the construction of the Dickson-Greinacher and Greinacher, respectively. All topologies possess rectification output proportional to the number of stages (N), and the main differences are related to the levels of derivation to reduce parasitic effects and the resulting power conversion efficiency (GARCIA-GARCIA, 2022).

Figure 5 – Other rectifier topologies: a) Dickson-Greinacher; b) Greinacher, c) Dickson, d) Full-Wave Dickson variation .



Source: Adapted from Garcia-Garcia (2022).

There are several topologies for converting alternating current (AC) to direct current (DC), and the choice of the appropriate topology depends on the design specifica-

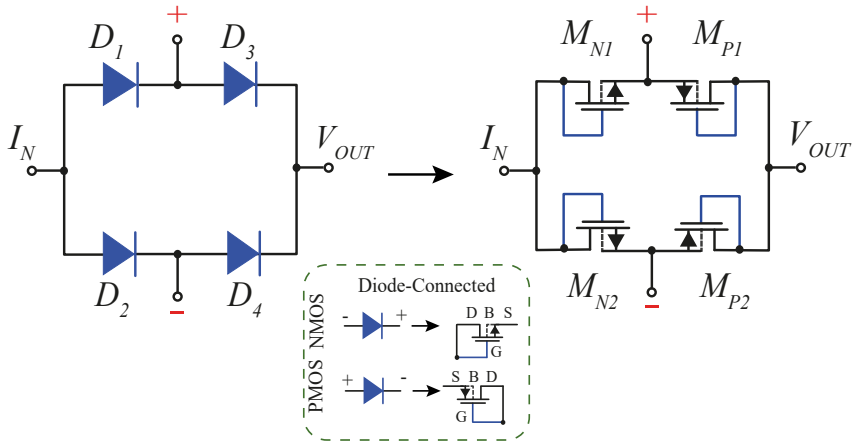
tions. RF signals present a time-varying input power. This study aims to convert radio frequency (RF) signals into DC with extremely low voltage levels. Thus, to fulfill the design requirements, the chosen topology must work efficiently even at low input power levels.

Therefore, utilizing conventional silicon diodes becomes inefficient at low input power ranges due to its direct bias voltage of 0.7 V, which results in a considerable conduction loss. An alternative to replace the conventional diode is the Schottky diode, which works at high frequencies and has a lower direct bias voltage in the range around to 0.25 V. However, the disadvantage of this semiconductor is the steps required for its fabrication. For large-scale productions, the Schottky diode becomes undesirable due to the requirement of manufacturing steps not normally available in traditional processes, as well as the associated high cost.

Thus, another option to replace diodes in rectifiers is to emulate them with CMOS (Complementary metal-oxide-semiconductor) transistors, which have a lower VT value (this value depends on the process adopted) and are efficient for low input powers. In addition, CMOS transistors also have a lower cost when produced on a large scale.

Figure 6 shows the full-wave configuration, where the diodes are replaced by CMOS transistors in diode-connected configuration. This would be a suitable option for RF-EH, however it is not very efficient. According to Lian et al. (2023) this topology has a high turn-off voltage due to the threshold voltage and also obtains a low PCE value for low input powers due to the forward voltage drop across the transistors. However, this topology is advantageous if you want to obtain a high PCE for high input power.

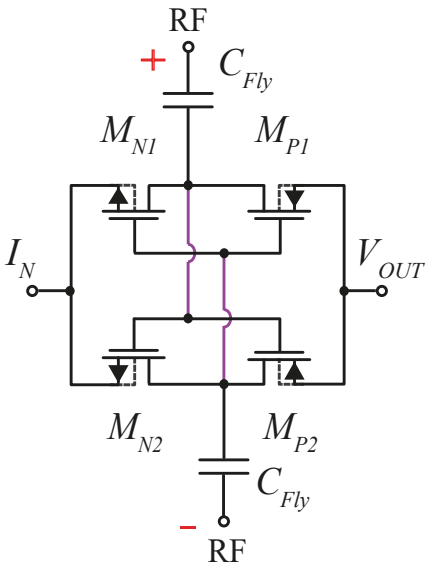
Figure 6 – Diode-connected configuration.



Source: Author.

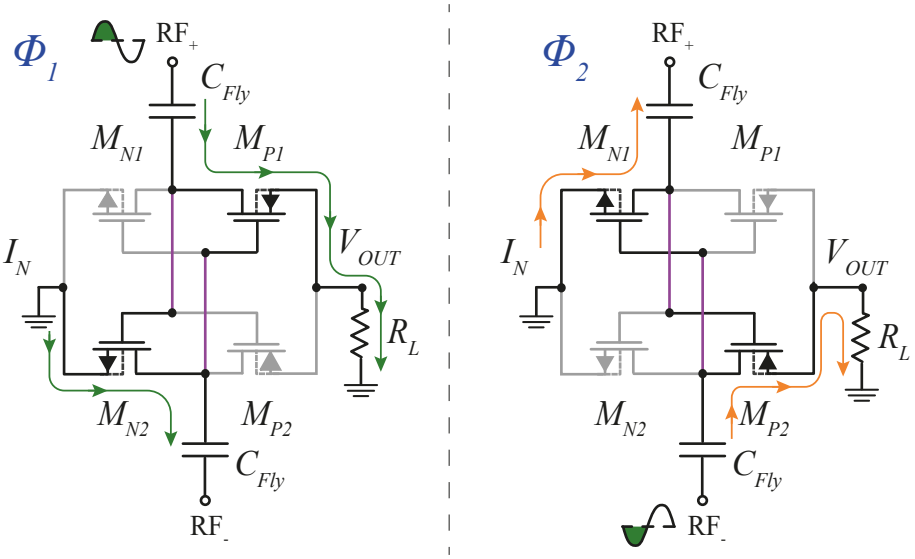
Thus, since the diode-connected configuration is not very suitable for low input power applications, a cross-coupled configuration (Figure 7) is an option, which in turn, according to (LIAN et al., 2023), achieves the maximum PCE at a low input power level. The Cross-Coupled topology driven by an RF differential input signal (CCDD - Cross

Figure 7 – Cross-Coupled Drive Differential rectifier.



Source: Author.

Figure 8 – 1° Stage CCDD rectifier operation principle.



Coupled Differential Drive), shown in Figure 7, was proposed by Kotani, Sasaki e Ito (2009), and this topology is based on a differentially driven active gate bias mechanism allowing a low ON resistance simultaneously with a lower leakage of the reverse current into the diode-connected MOS transistors. In this work, a PCE of 67.5% and a sensitivity of -12.5 dBm were obtained, considering a single stage, a 10 kΩ load, RF signal frequency of 953 MHz, and a 180-nm CMOS process. Also, according to Tran, Cha e Park (2017) this topology is widely used due to its low leakage current and its potential for further modification depending on the application.

Several other papers also adopt the CCDD configuration for RF-EH. In Martins e Serdijn (2021) the CCDD configuration is used without any modification, and only one

stage,operating over a wide input power range from -24 to +15 dBm. The system has been designed considering the 180 nm CMOS process and the RF frequency of 403.5 MHz.

The work of Al-Absi et al. (2021) proposes a modification in CCDD via an adaptive body bias technique to decrease the VTH of the transistor when PMOS is triggered. In addition, the technique further aims to minimize the current flow in the reverse bias condition when PMOS is off by increasing its VTH. The design used the 180-nm CMOS process, 953 MHz RF frequency, and achieved PCE of 78.2% for a sensitivity of -27.5 dBm for 100 kΩ load.

In, Oliveira (2022) the CCDD is also used without modification. A methodology based on output voltage maximization of transistor sizing in CCDD configuration for ultra-low voltage operation is demonstrated, as well as a comparison between one, three, and five rectifier stages with improved PCE performance and sensitivity. In this study, it is seen that the adoption of one rectifier stage is sufficient for conversion at ultra-low operation with low input power. The technology used was 180 nm CMOS and an RF frequency of 915 MHz.

Figure 8 shows the operation of the rectifier operating in only one rectification stage, so when the signal is in the positive semi-cycle, transistors M_{P1} and M_{N2} are in conduction, charging the capacitor C_{Fly} connected to the negative input, and the others are reversely biased, reducing the leakage current. In the second stage, where the signal is in the negative half cycle, transistors M_{P2} and M_{N2} are conducting, while the others are reversely biased, discharging C_{Fly} from the negative input, and charging C_{Fly} from the positive input. The threshold voltage of the transistors is still reduced when they are conducting due to the differential input.

Furthermore, in the work by Chong et al. (2021), the CCDD rectifier is used in two input capacitor coupling configurations. In this study, the CCDD rectifier demonstrates a wide dynamic range (DR) at PCE and employs the self-biasing technique to reduce direct VTH. In addition, diode-connected MOSFETs are used to control the reverse leakage current and improve the direct current. The SCC-CCDD and ICC-CCDD rectifiers are fabricated in 130-nm CMOS and exhibit a DR of 13 and 14.5 dB, respectively, for a PCE greater than 40%. In an alternative analysis, the SCC-CCDD achieves a maximum PCE of 83.7% with a sensitivity of -19.2 dBm at 1 V, while the ICC-CCDD achieves a maximum PCE of 80.3% with a sensitivity of -18.7 dBm.

Recent work shows modified CCDD configuration to increase the power dynamic range (PDR), i.e. to obtain an optimal PCE even with varying sensitivity. (CHOO et al., 2023) proposes an advanced topology amalgamation technique to increase the PDR and significantly improve the PCE. This work addresses adaptive DC counter deactivation in the last phase of the rectifier by means of an auto-biasing configuration. The design was developed using 65-nm CMOS technology at two different frequencies. The first frequency is 900 MHz, operating at an ultra-low voltage of about 0.2 V, presenting a wide PDR

(power gain) of 21 dB. The second frequency is 1.8 GHz, operating at about 0.4 V, with a wide PDR of 15 dB. The peak PCE values are 79.77% and 51.3%, respectively, under a 100 kΩ load.

Li et al. (2022) also presents a proposed rectifier to increase the PDR by using a dual path with adaptive control circuits. In this context, two rectifiers are designed: one modified CCDD and one fully NMOS. This approach allows selecting the desired path, i.e., the high-power path or the low-power path, according to the input power level. The design is implemented in a 180 nm CMOS process, considering an RF frequency of 2.45 GHz, achieving a sensitivity of -20.7 dBm for an output voltage of 1 V. Furthermore, the PCE range above 20% of the proposed RF-EH is kept between -22 dBm and 5 dBm, with a total range of 27 dB. Two peak PCEs, 57% and 62%, are observed for input powers of -15 dBm and 1.6 dBm, respectively.

Thus, there are several options for the rectifier implementation in the RF-EH design, as shown in Table 3. However, the choice of the basic topology and the possibility to modify its configuration depend on the specifications of each particular application. Current studies have shown that the rectifier is the most crucial component in RF-EH design, and its design presents several challenges. Furthermore, a trend towards designs operating at an ultra-low voltage of 0.4 V is observed in Table 3 and Figure 9, with newer technologies. However, a low peak PCE value is still observed. There is also no approach using frequencies of 5.8 GHz or higher with fully CMOS topologies. With this, it is possible to conclude that the exploitation of the rectifier is fundamental to innovate in an RF-EH system, with a high efficiency of energy conversion.

Figure 9 – Voltage output and sensibility comparison of state-of-the-art on Table 3.

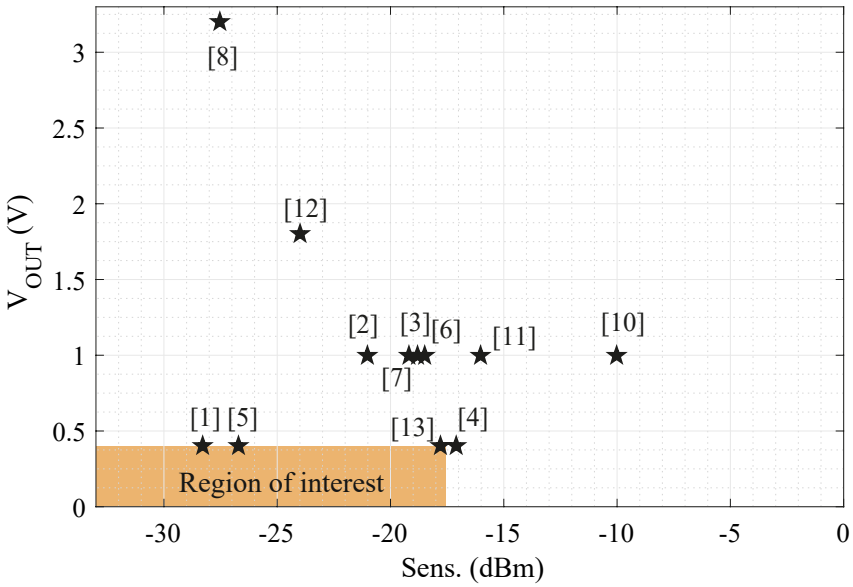


Table 3 – State-of-the-art of CCDD rectifiers topologies.

Ref.	Tech. (nm)	Freq. (MHz)	N° Stag.	R_L (kΩ)	V_{OUT} (V)	Sens. (dBm)	Peak PCE (%)
[1] TCASII	28	2450	2	⋆	0.4	-28.3	31.1
[2] Electronics$^{\triangle}$	65	900	(3 + 2)$^{\diamond}$	100	1	-21	88.7
[3] Sensors	65	900	-	100	1	-18.8	73
[4] JSSC	65	2450	1	⋆	0.4	- 17.1	48.3
[5] JSSC	65	2450	1	⋆	0.4	-26.7	32.3
[6] VLSI	65	900	5	1000	1	-18.5	19.1
[7] TCASII	130	900	3	100	1	-19.2/-18.7	83.7/80.3
[8] ACESS	180	953	5	100	3.2	-27.5	78.2
[9] JSSC	180	953	-	10	-	-12.5	67
[10] OJCS	180	1050	3	10	1	-10	45
[11] ESSCIRC	180	918	1-2-4	1000	1	-16	45
[12] TCASI	180	403	1	⋆	1.8	-24	40.2
[13] JSSC	180	915	12	⋆	0.4-2.2	-17.8	34

$^{\triangle}$ CCDD Hybrid Reconfigurable, ⋆ MPPT PMU, $^{\diamond}$ 3 main + 2 auxiliary rectifiers

[1] - Xu, Flandre e Bol (2023), [2] - Lian et al. (2023), [3] - Alhoshany (2022), [4] - Xu, Flandre e Bol (2019), [5] - Xu, Flandre e Bol (2021), [6] - Lian et al. (2022), [7] - Chong et al. (2021), [8] - Al-Absi et al. (2021), [9] - Kotani, Sasaki e Ito (2009), [10] - Xu et al. (2022), [11] - Yan, Kuo e Liao (2022), [12] - Martins e Serdijn (2021), [13] - Zeng et al. (2019).

2.1.2 IMPEDANCE MATCHING NETWORK

Power conversion efficiency and sensitivity, which are parameters related to the input power, are the main results to be analyzed and achieved in an RF-EH design to determine its effectiveness. However, another challenge of this design is to ensure that the maximum transfer of the RF signal captured by the receiving antenna to the end load occurs.

A transmitting or receiving antenna has a characteristic impedance, which is determined by its physical elements, size, shape, and design characteristics. Impedance is a measure of the resistance offered by the circuit to the flow of alternating current.

On the other hand, the device or system connected to the antenna, such as the rectifier in our case, also has its own characteristic impedance, which is measured after all circuit sizing is completed. However, to maximize the power transfer between the antenna and the device, it is desirable that the impedance of the antenna must be equal to the impedance of the device. When there is an impedance mismatch between the antenna and the device, some of the signal power is reflected back to the antenna. These power reflections can cause a decrease in the efficiency and performance of the antenna, as well as the overall performance and efficiency of the RF-EH system.

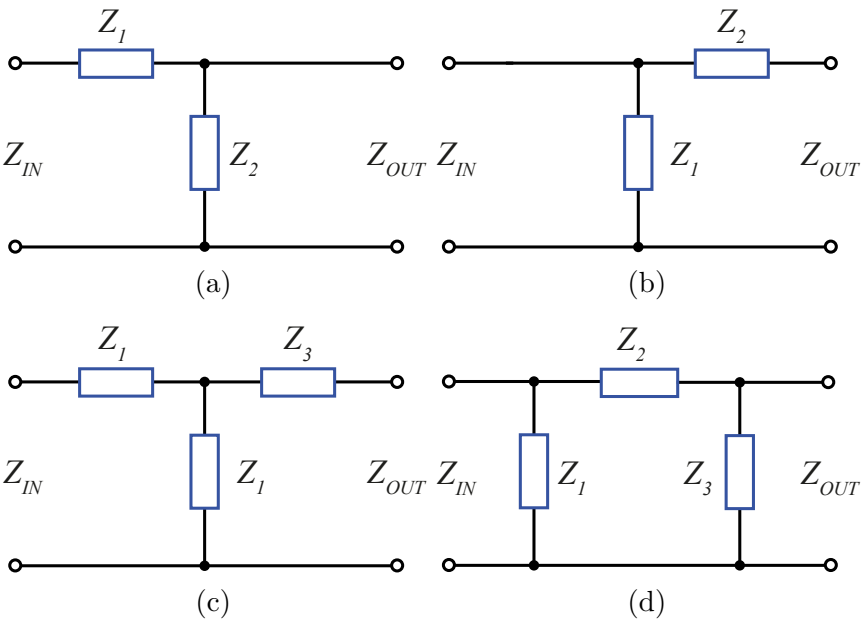
To achieve impedance matching, different techniques and components can be used,

including impedance transformers, transmission lines, LC circuits, among others. These elements are designed to adjust the antenna impedance to align with the impedance of the device. This leads to the maximization of power transfer and the minimization of reflections.

In this subsection, impedance matching techniques applied to integrated circuits will be discussed, with a special focus on RF-EH systems.

According to Tran, Cha e Park (2017), impedance matching can be represented by three basic configurations: L, T, and π, as illustrated in Figure 10.

Figure 10 – Configuration Impedance Matching Network, a) L Network; b) Reversed L Network; c) T Network; d) π Network.



Adapted from (TRAN; CHA; PARK, 2017).

Among these configurations, the L-Network configuration is widely adopted in RF-EH applications due to its simplicity. It typically consists of only two passive components (an inductor and a capacitor), making it easy to adjust to meet design requirements. Additionally, this configuration is versatile and can be applied across various frequency ranges, which makes it a popular choice in RF-EH systems.

In addition, the L-matching network can be customized to meet the requirements of each design. The study conducted by Mohan, Sahoo e Mondal (2022) employs a three-stage tunable impedance matching method that aims to maximize the power transfer from an RF source operating at a frequency of 953 MHz. The proposed scheme intends to eliminate the necessity of complex implementations, such as capacitor banks and large inductors. Through the utilization of this technique, a PCE of 51% was achieved with a sensitivity of -12 dBm.

In Liu et al. (2018), the RF-DC converter is implemented using an adaptive

impedance matching network. This allows for accommodating a wide range of input RF power variations and expanding the operating frequency range. Measurement results demonstrate that the impedance tuning mechanism can extend the optimal frequency range, where the efficiency exceeds 80% of its peak value, from 150 MHz (800-950 MHz) to 220 MHz (780 MHz-1 GHz) when the impedance is adjusted using the control circuitry.

Table 4 – State-of-the-art on IMN topologies of RF-EH.

Ref.	Tech. (nm)	Freq. (MHz)	Off-Chip Components	IMN Strategy	R_L (kΩ)	Sens. (dBm)	Peak PCE (%)
[1] VLSI	130	915	Inductors	Adaptive	10	-12.3	29.3
[2] TCASII	180	953	Inductors	Tunable	10	-10	65
[3] Sensors	180	900/2400	All ▷	Standard*	100	-17	67.1
[4] Energies	180	433	Inductors	Tunable	⋆	-13.6	49.06
[5] Sensors	180	2400	None	Standard	-	-14.1	21.15
[6] TCASI	180	403	Inductors	Adaptive	⋆	-24	40.2

⋆ MPPT PMU, * Dual-band, ▷ Capacitors and Inductors.

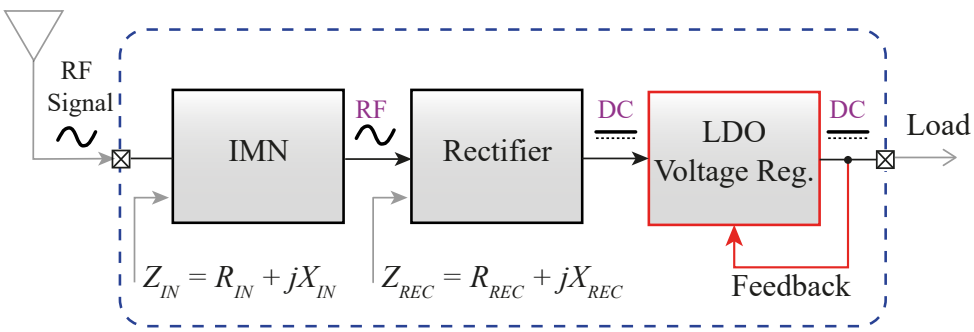
[1] - Liu et al. (2018), [2] - Mohan e Mondal (2021), [3] - Heo e Kwon (2021), [4] - Chen, Sun e Tsai (2022), [5] - Churchill et al. (2022), [6] Martins e Serdijn (2021)

2.2 VOLTAGE REGULATION

A voltage regulator is defined as a circuit that keeps the output voltage constant even if there are variations in input or output current. Therefore, in this work, our objective is to supply of to power devices that operate with fixed power supply, that is, with constant voltage source. For this, although the RF-DC conversion occurs, it is still necessary to add a voltage regulator, since the RF signal power varies according to the intensity of the collected signal.

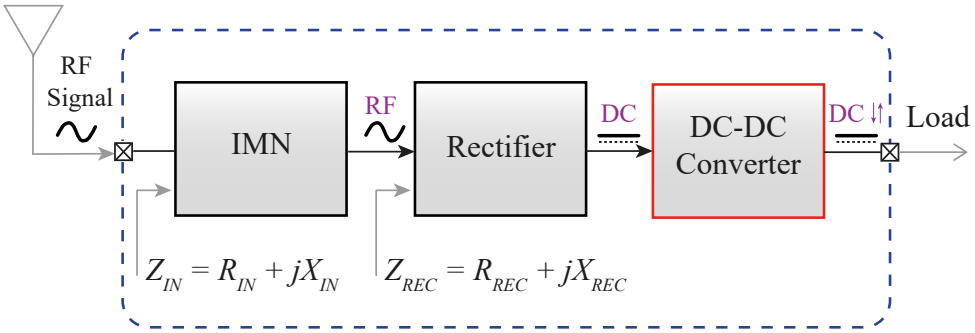
In RF-EH systems, the voltage can be regulated by three typical ways. The first is through a Low-Dropout Regulator (LDO), as shown in Figure 11.

Figure 11 – RF-EH system with LDO Voltage Regulation.



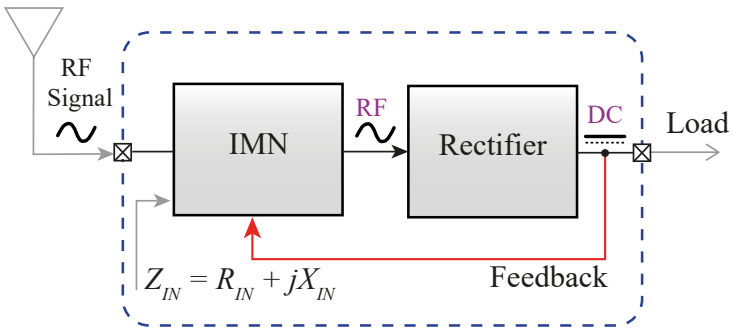
The implementation of a Low-Dropout Regulator (LDO) in the energy harvesting system is due to its easy implementation in integrated circuits to regulate the voltage, Figure 11 illustrates this application. However, this type of approach has limited energy efficiency due to the power loss of the dropout voltage, and requires the rectifier output voltage to be higher than the application output voltage, which in this case is 0.4 V. Therefore, for the ultra-low power RF-EH system for batteryless applications, the use of this type of regulation is a disadvantage, as we are looking for a low input power, and this type of technique requires high sensitivity, as well as the value of the rectifier output necessarily always being higher than the desired value.

Figure 12 – RF-EH system with DC-DC Converter.



Another alternative for regulating the voltage to a desired value is to use a DC-DC converter at the output of the rectifier, as shown in the Figure 12. The advantage of this application is that it is independent of the variation in input power, so it allows the voltage to be adapted to the desired specification. Thus, this type of system usually has high efficiency in voltage conversion, and has the characteristic of maintaining the stability of the converted value, in addition, it also allows precise control of V_{OUT}, by means of feedback circuits, so regulation can be achieved for a restricted range of values. Depending on the application requirements, DC-DC converters can also increase or reduce the V_{OUT} value, allowing operation with low and ultra-low voltages.

Figure 13 – RF-EH system with Closed-loop Voltage Regulation through adaptive impedance matching.



Finally, from Figure 13 another alternative for implementing RF-EH system regulation can be through the implementation of closed-loop voltage regulation. In this approach, the system PCE only occurs at low sensitivity levels, without the need to generate output voltage levels higher than the desired ultra-low value. Therefore, in order to be able to adjust the impedance matching value, the rectifier output voltage is compared with a voltage reference, so that the specified level is maintained.

Since the main specification of this work is the conversion of the RF signal to a fixed voltage value of 0.4 V, starting from low sensitivity values, in order to power batteryless devices, an adaptive impedance matching control approach will be considered.

As there is no requirement for the system to be efficient over the entire input power range, the use of a DC-DC converter, which is the most conventional method but also the most complex, is not necessary in the application of this work. As for the first technique, presented using an LDO, the main bottleneck would be that the input power level must always be higher in order for regulation to take place, which generates an output voltage that is always higher than 0.4 V, and also low conversion efficiency due to the dropout voltage, thus failing to meet the specifications of this design.

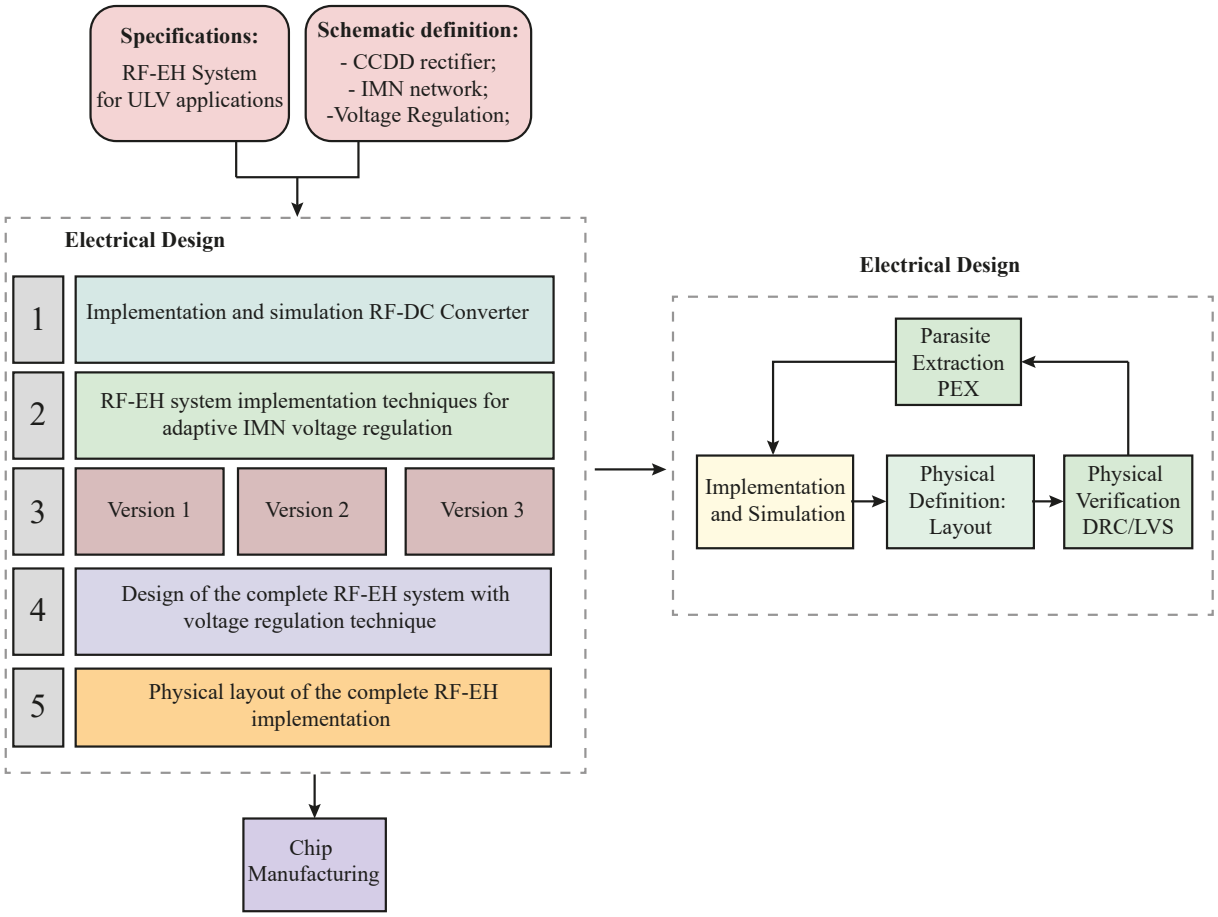
3 DESIGN METHODOLOGY

The design flow for RF Energy Harvesting is shown in Figure 14. Thus, following a conventional design flow for analog integrated circuits, the project specifications are initially defined, where the objective is to design the RF-EH for the final application. Subsequently, a study of the literature is carried out, in which the relevance of each circuit to be designed and its functionalities are understood. The schematic of each circuit that makes up the RF-EH is then defined, according to the specifications previously defined.

From this data, we move on to the electrical design, where in this work we first implement and simulate the RF-DC converter, then implement the impedance matching adaptation techniques to keep the RF-EH system with a regulated output voltage, then the complete RF-EH design with the voltage regulation technique and finally the physical layout of the complete RF-EH system.

The electrical design process applied in this work follows the flow of implementation and simulation, layout design, physical verification of the layout (layout versus schematic (LVS) and design rule check (DRC)) and parasitic extraction (PEX). To carry out this design flow, the Cadence Design Systems tools virtuoso and spectre were used for simulations and calculations, and the Siemens Calibre tool was used for the physical checks.

Figure 14 – RF-EH design flow.



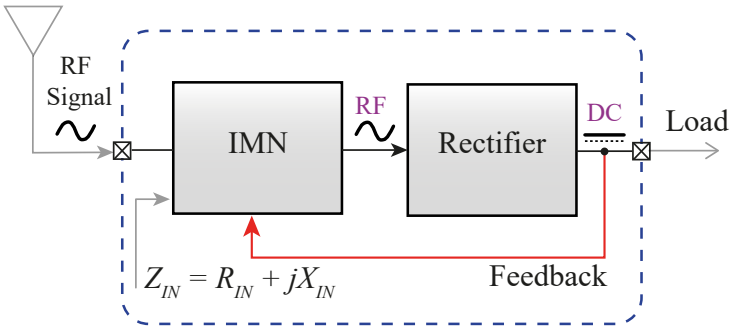
The electrical design flow is only finalized when the initial design specifications are met, and so the chip is sent for manufacturing.

In the following chapters, this design flow is followed and shows final results with good performance that meet the design specifications previously presented in Chapter 1 of this work.

4 RF-EH SYSTEM IMPLEMENTATION TECHNIQUES

Based on the definition of the RF-EH system application in batteryless devices operating at ULV, the closed-loop regulation technique using adaptive impedance-matching control was chosen. As presented in the study carried out previously in Section 2.2, Figure 15 shows the regulation through negative feedback in a generic way. This chapter presents three versions of the proposed implementation of the complete RF-EH system for batteryless applications, addressing its main advantages and challenges.

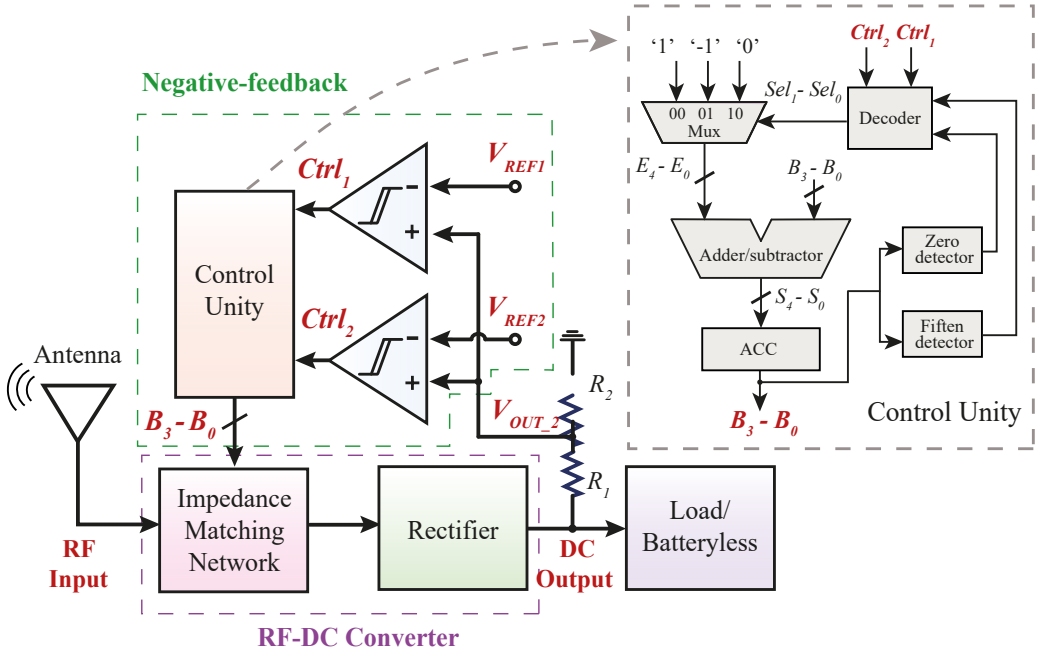
Figure 15 – RF-EH system with Closed-loop Voltage Regulation through adaptive impedance matching.



4.1 RF-EH VERSION 1 - MIXED-CIRCUIT DIGITAL-ANALOG AND RF

The first version of voltage regulation through adaptive control of impedance matching is carried out considering a mixed analog-digital and RF system, which can be

Figure 16 – Block diagram of the complete RF-EH system with mixed digital-analog and RF voltage regulation.



seen in Figure 16. Its implementation is realized considering a 180-nm CMOS process.

4.1.1 RF-DC CONVERTER VERSION 1

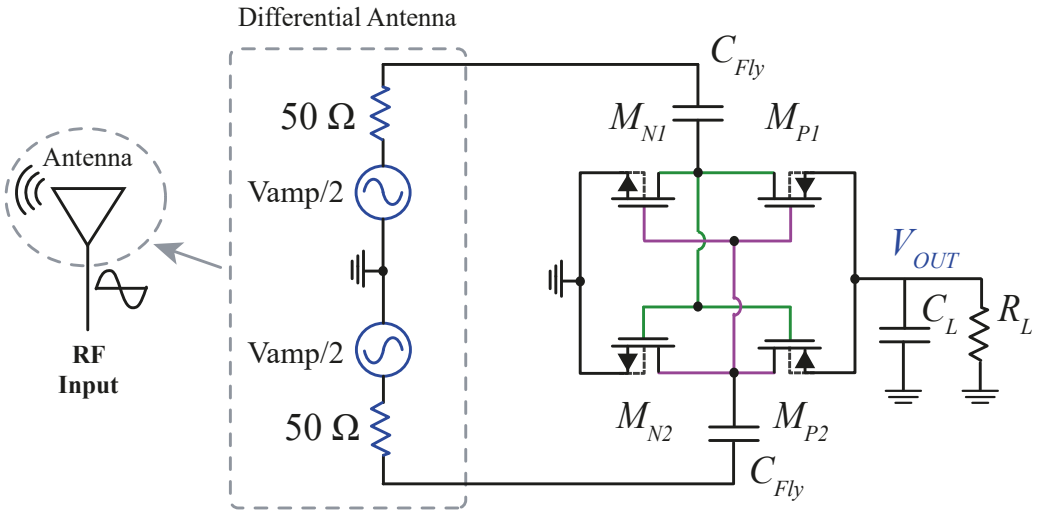
For the first stage of the RF-EH, shown in Fig. 16, in which the signal is harvested and converted into DC, the first block to be developed is the rectifier. After signal conversion, an impedance-matching circuit is designed to ensure maximum power transfer.

The following subsections discuss the methodologies for designing the rectifier circuit and the impedance-matching network.

4.1.1.1 RECTIFIER VERSION 1

As described in Chapter 2, the rectifier is the main block of the RF-EH system, being responsible for the RF to DC conversion. Thus, due to its relevance in the system, this is the first block to be designed.

Figure 17 – CCDD Rectifier topology.



The rectifier implementation considers the conventional single-stage Cross-Coupled Differential Drive (CCDD) topology used by Kotani, Sasaki e Ito (2009) because it is a topology that has a high PCE value when considering low values of RF signal input power. According to Oliveira (2022), when using the CCDD topology for ultra-low voltage operation, only one rectification stage is enough to obtain the maximum output voltage and a high PCE value. Thus, this circuit (Figure 17) consists of two NMOS-type transistors (M_{N1} and M_{N2}) and two PMOS-type transistors (M_{P1} and M_{P2}) operating as diodes, two flying capacitors (C_{Fly}), a filtering capacitor (C_L) and a resistive load (RL) to emulate the application load. In addition, to reduce the values of parasitic capacitance in ULV operations, the low-VT transistors with the minimum channel length ($L_{P1} = L_{P2} = 250$ nm and $L_{N1} = L_{N2} = 300$ nm) are considered.

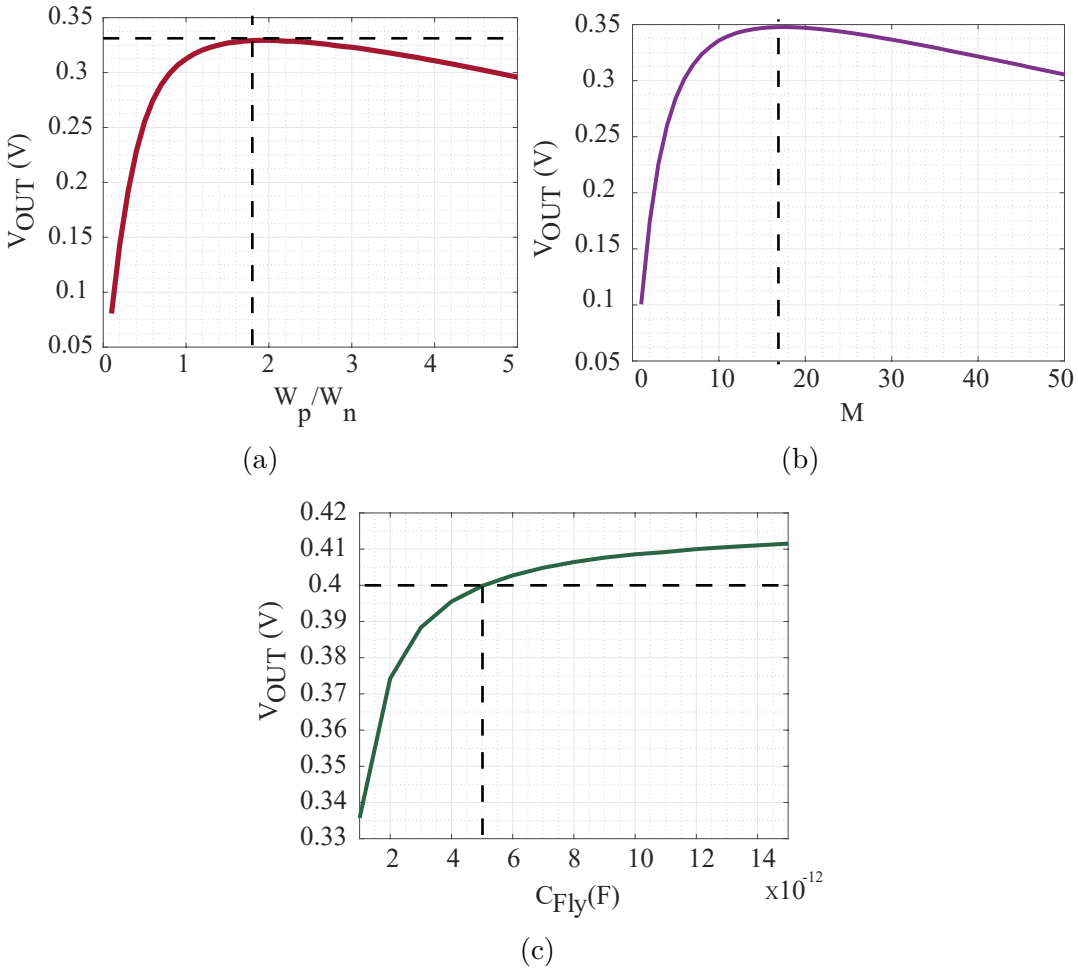
For the sizing of the transistor channel widths (W_{P1}, W_{P2}, W_{N2} and W_{N2}) and also the values of the capacitors C_{Fly}, an iterative design methodology is considered with

the aim of maximizing the DC level of the output voltage, considering a fixed input RF voltage signal. This approach aims to improve sensitivity and PCE.

The rectifier sizing also considers the output load analysis, in which the load of 10 and 100 kΩ, respectively, were adopted.

The channel width values were then parametrically analyzed and, as can be seen in Figures 18a and 18b, the results that give the maximum output voltage are W_{P1}, W_{P2} = 1.6 μm, W_{N2} and W_{N2} = 1 μm, with 18 multipliers. A parametric analysis of the flying capacitor was also carried out, as shown in Figure 18c where C_{Fly} = 5 pF was obtained, where this value could be higher, however from 5 pF it is necessary to have a large increase in C_{Fly} to obtain a small increase in V_{OUT}.

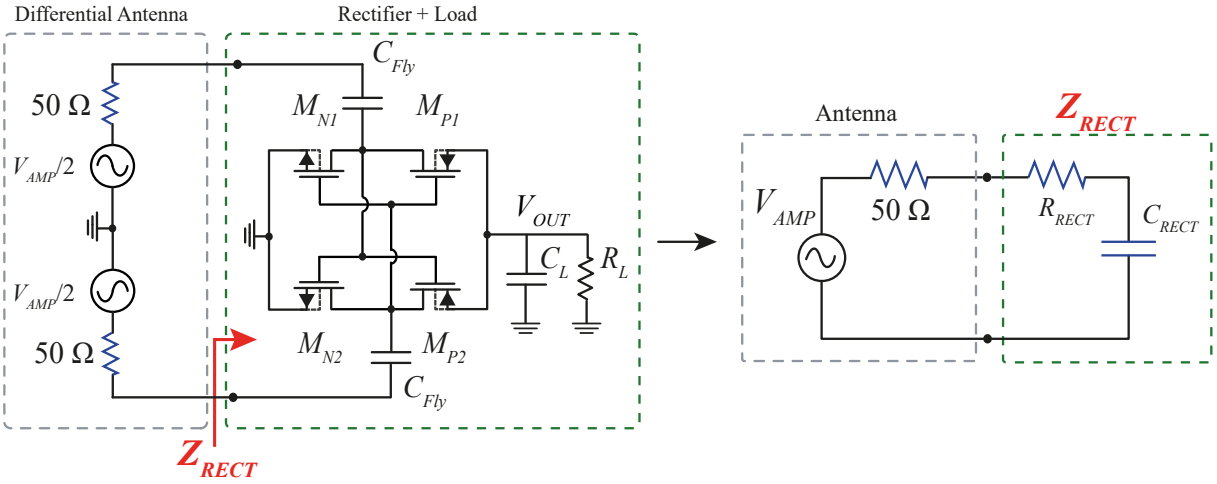
Figure 18 – Rectifier sizing methodology: 18a Variation W_p/W_n in function V_{OUT}; 18b Variation multipliers in function V_{OUT}. 18c Variation capacitance C_{Fly} in function V_{OUT}.



4.1.1.2 RECTIFIER INPUT IMPEDANCE VERSION 1

After sizing the elements in the CCDD topology, in RF circuits it is essential to consider the concept of maximum power transfer (MPT) from the receiving antenna to

Figure 19 – Obtaining rectifier input impedance.



the end device, as explained in the chapters 1 and 2. When this condition is not met, the circuit does not operate at maximum efficiency, resulting in a reflection portion of the signal. It is therefore essential to measure the rectifier's impedance in order to minimize reflection losses and guarantee the best system performance. The CCDD rectifier is not a linear circuit, but according to Martins (2021) its input impedance can be approximated by a linear value.

Thus, the input impedance of the rectifier can be represented by Equation 4.1, where Z_{RECT} is a complex value and is defined by R_{RECT} which represents the input resistance and X_{RECT} which represents the input reactance. Thus, to measure the impedance of the rectifier circuit (Z_{RECT}), the R-C representation of the rectifier is considered. To measure the values of R and C, we use harmonic balance (HB) analysis under permanent regime conditions.

$$Z_{RECT} = R_{RECT} + jX_{RECT} \tag{4.1}$$

From this analysis, it is possible to represent the rectifier circuit as an R-C equivalent circuit, given that $X_C = 1/\mathrm{j}\omega\mathrm{C}$, as shown in Figure 19, and the results are $R_{RECT} = 372.1\ \Omega$ and $C_{RECT} = 165.6$ fF.

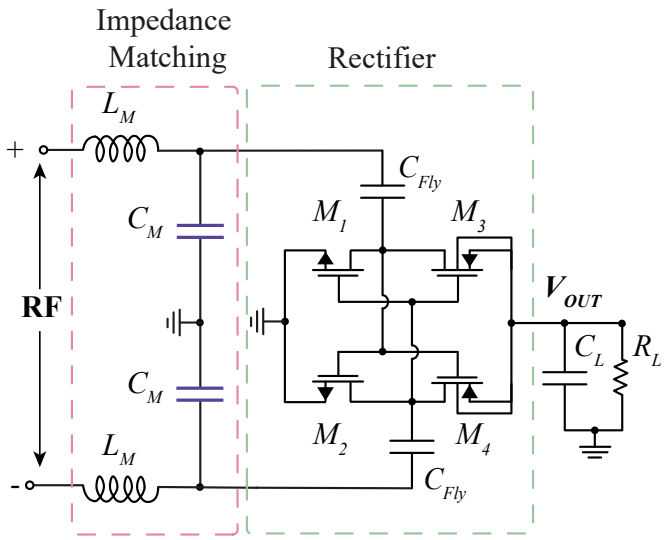
4.1.1.3 IMPEDANCE MATCHING NETWORK VERSION 1

To represent the differential antenna, this work considers as inputs two PORT sources of 50 Ω, a standard value for antennas. Thus, after measuring Z_{RECT}, an impedance difference is observed in relation to the PORT. In order to guarantee the MPPT and maximum PCE of the RF-EH system, it is necessary to design an impedance matching network (IMN).

To do this, as mentioned in Chapter 2, session 2.1.2, there are impedance matching techniques, and the Smith chart method is used to obtain the IMN equivalent circuit.

Thus, for the design of the IMN, the L-C network strategy was obtaining, illustrated in Figure 20. The values of L-C are $L_M = 70$ nH and $C_M = 280$ fF.

Figure 20 – Schematics of the RF-DC Converter with Impedance Matching L-C Network.



As can be seen, the inductor has a higher value to be integrated, so in this topology, it can be implemented off-chip.

After obtaining the impedance matching network configuration L and the values of the concentrated elements L and C, obtained using the Smith Chart, we proceeded to test this configuration together with the rectifier circuit. The HB analysis carried out previously, which allowed us to obtain Z_{RECT}, can also be applied again to check whether Z_{RECT} with the matching circuit has reached the desired Z_0 value (50 Ω).

At this stage of the design, there is an RF-EH that correctly collects and converts to an ultra-low voltage, and so far only a fixed input voltage value has been considered to simulate the RF signal. However, in real situations, the RF signal varies in amplitude. A technique for regulating the output voltage is therefore explored, in order to keep the signal fixed at 0.4 V, regardless of the variation in the amplitude of the input signal.

The work by Liu et al. (2018) adopts the concept of adaptive impedance matching, using the perturbation and observation technique for this purpose. Thus, the adaptive capacitor is realized through the implementation of a digital control loop, and is implemented using a 4-bit capacitive matrix. Based on this study, the adoption of adaptive impedance matching is proposed in this work. The next step is to analyze which of the two elements present in the impedance matching can be varied and controlled.

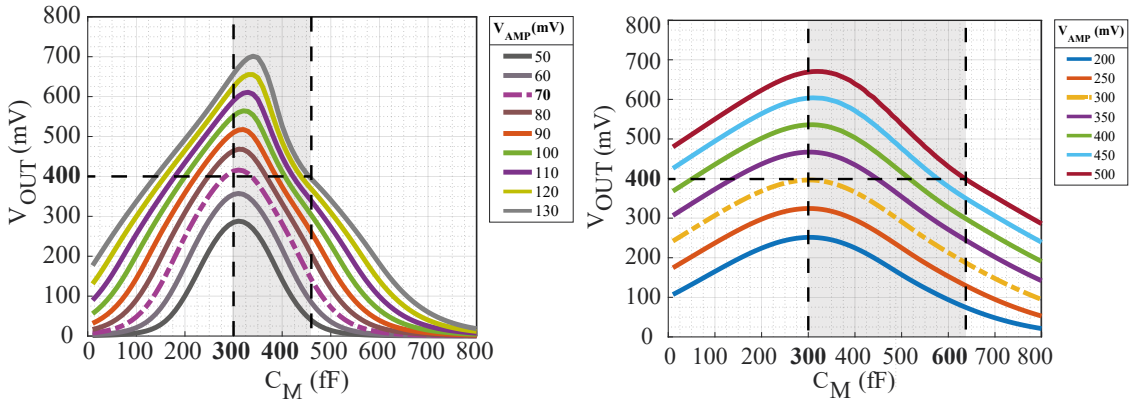
4.1.1.4 ADAPTIVE IMPEDANCE MATCHING NETWORK VERSION 1

With the values obtained for L and C, we can see the area they will occupy. Thus, only the capacitor can be implemented using the CMOS process. It can also be seen that adapting a capacitor to be controlled is simpler than adapting an inductor. A capacitor is implemented by joining two thin metallic plates separated by a dielectric, while an inductor is formed by a wire coiled in a spiral, where there is a greater challenge in terms of the area occupied and the precision of implementation, making it more complex to adapt than a capacitor.

Therefore, the variable nature of the RF signal is taken into account and an analysis is made of the range of capacitance values that keep the output voltage fixed at 0.4 V, as shown in Figure 21b. This analysis considers a variation in the amplitude of the RF signal V_{amp} from 50 mV to 130 mV, and it can be seen that from a minimum voltage of 70 mV, there is a range of capacitance values around 300 fF to 470 fF which maintains the output voltage value as specified.

Once this capacitance variation has been carried out, considering the minimum and maximum values of the range obtained, which keeps the output voltage fixed at 0.4 V, it is proposed to use a 4-bit programmable capacitive bank as illustrated in Figure 22.

Figure 21 – Variation of the DC output voltage as a function of the matching capacitor: (a) $R_L = 10$ kΩ; (b) $R_L = 1$ kΩ.



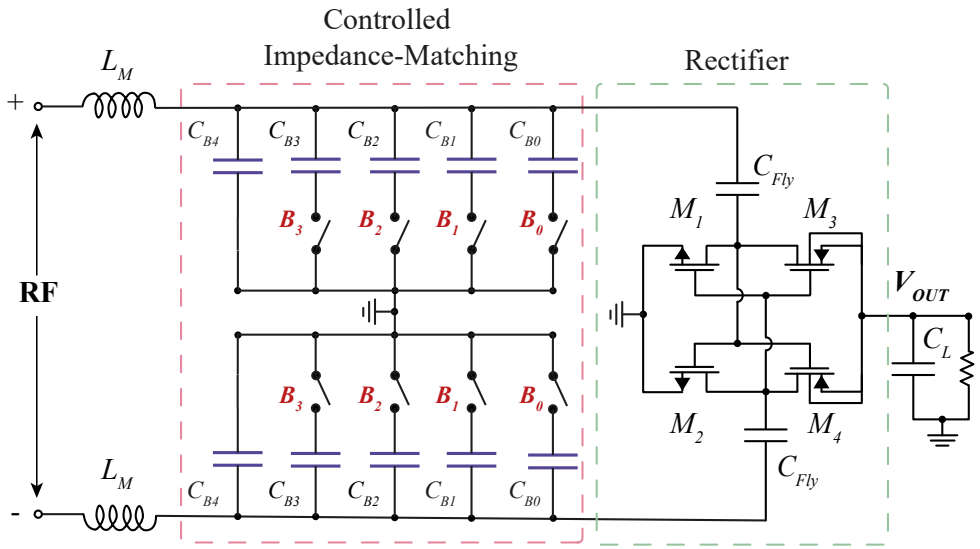
(a) (b)

4.1.2 CLOSED-LOOP VOLTAGE REGULATION VERSION 1

Initially, the methodology for implementing the closed-loop system is based on comparing the DC output voltage with two reference values. Thus, a digital counter was implemented to change the values of the programmable capacitor in order to maintain the output voltage level.

So, the first reference of the comparison is the measurement of the V_{OUT} level by means of a resistive divider composed of R_1 and R_2, equal to 1 MΩ.

Figure 22 – Implementation of a 4-bit programmable capacitive bank.



In this first case, two comparators were used with a reference voltage equal to 0.2 + Δ and 0.2 - Δ, respectively. Where, Δ is the hysteresis control parameter that defines the expected range for the output voltage. The value of Δ is defined to 10 mV, to obtain a 10% range around 0.4 V. The topology implemented for the comparators in this work is the pseudo-differential amplifier, as shown in Figure 24, with according Compassi-Severo e Noije (2019) is a good candidate for ULV operations.

The comparison logic consists of the output values of the comparators $Ctlr_1$ and $Ctrl_2$, the counter must increment, decrement or maintain the values of the capacitor control signal, according to Table 5.

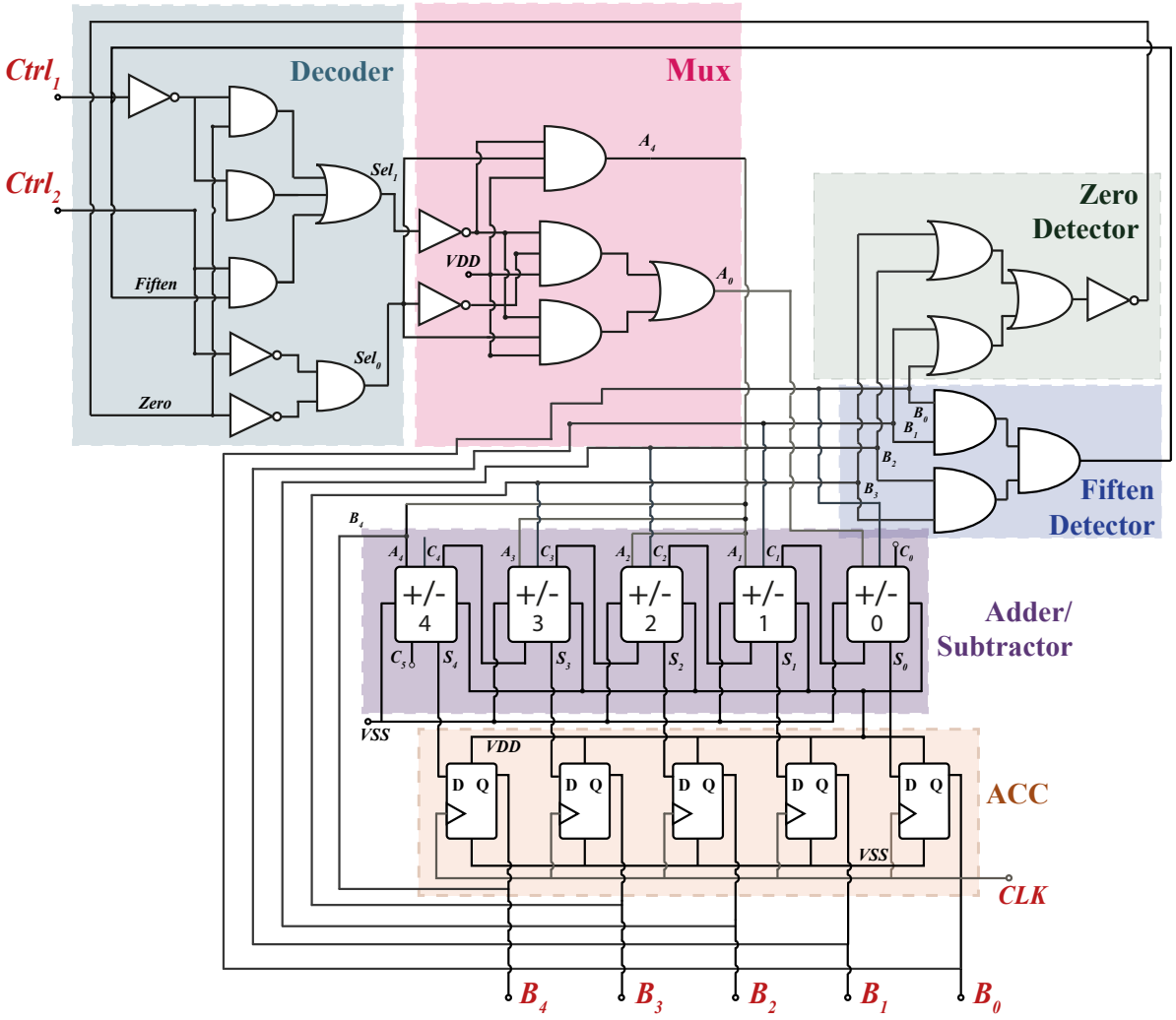
After performing the comparison of the rectifier output voltage, the flow of this design goes to the control logic unit proposed for this work.

The control unit illustrated in Figure 23 basically consisted of a four-bit adder and an accumulator (ACC) that manages the four-bit word ($B_0 - B_3$) used to adjust the value of the capacitor C_M. One of the inputs of the adder is connected to $B_0 - B_3$ and the other is a constant value ($E_0 - E_3$), set by the multiplexer. The constant value can be equal to 1, -1 and 0 (decimal) to increment, decrement or hold the value of $B_0 - B_3$ respectively. The mux selection bits Sel_0 and Sel_1 are obtained with a decoder block. The decoder has as inputs the outputs of the comparator signals ($Ctlr_1$ and $Ctrl_2$) and the outputs of the zero detection and fifteen detection blocks, which are used to avoid overflow and underflow in the four-bit word of the capacitor.

Table 5 – Comparison logic for closed-loop regulation with digital control.

$Vout_{div}$	$Ctlr_1$	$Ctlr_2$	**Action**
$< 0.2 + \Delta$	0	0	Decrements
$0.2 + \Delta$	0	1	Never Happens
0.2 - Δ	1	0	Retain
> 0.2 - Δ	1	1	Increment

Figure 23 – Control Unit implementation.

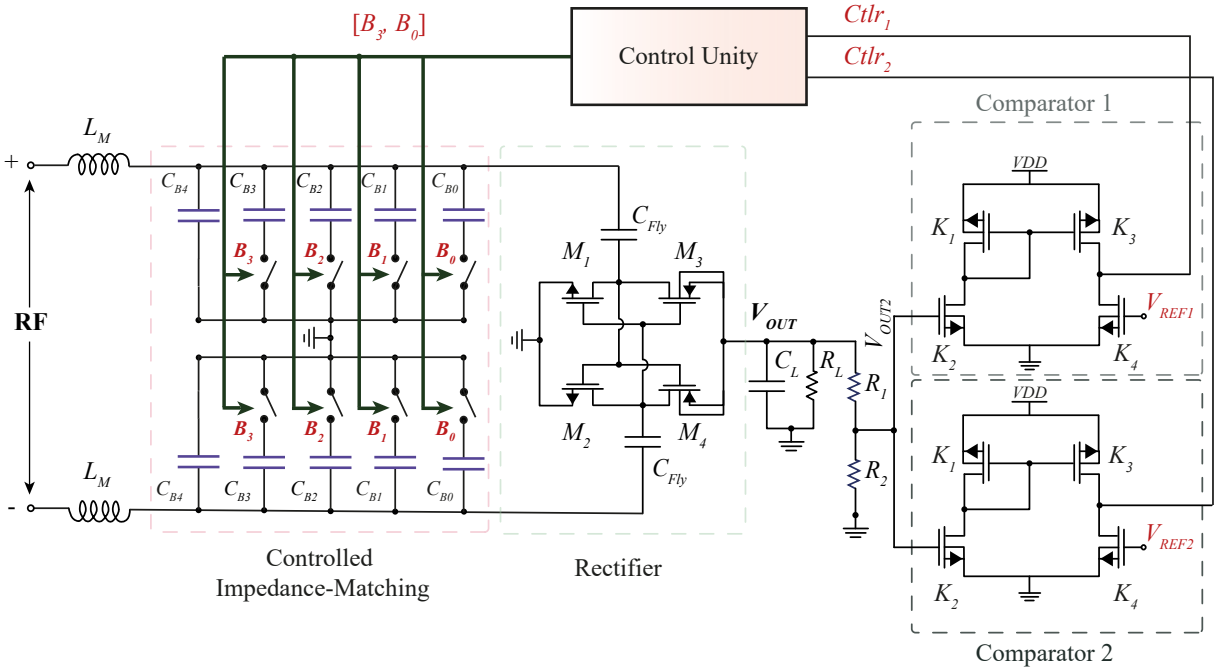


Finally, the first version of the RF-EH system is illustrated in Figure 24. All digital circuits have been implemented with customized CMOS static gates, designed to operate with a V_{DD} value of 0.4 V. The clock signal and voltage references are considered as external signals.

Simulations of the complete system when the input RF signal has amplitudes of 70 mV, 140 mV, 210 mV, 280 mV, 350 mV, 420 mV and 490 mV, and an output load of 10 kΩ can be seen in Figure 25. It can be seen that the system self-regulates to the desired output voltage at the lowest input level of 70 mV. An input power of 24.22 μW, an output power of 17.11 μW and a digital circuit power of approximately 1.7 μW (using a clock frequency of 457.5 MHz) were observed.

The PCE of the complete system can be calculated using Equation 1.2 in section 1.1. For the first version of the RF-EH, Figures 26b and 26a depict the PCE and the output voltage as a function of the input power. It can be seen that the sensitivity of the proposed system reaches a level of -16.12 dBm. This parameter is defined as the minimum power level required to obtain the desired output voltage level. The maximum PCE obtained at the power level at which the output voltage reaches 0.4 V is 67.29 % (where the clock

Figure 24 – Complete RF-EH system for the first version with 180-nm. Digital clock signal, not shown.



generator is not considered in the calculation).

Due to the unavailability of the 180-nm process for academic purposes, using the Europractice service, we should move the circuit implementation to another process. We have chosen the 65-nm process due to its good cost-benefit ratio and also to its size, since, for ultra-low voltage designs, the minimum value of the channel width is used through Low-VT transistors.

Figure 25 – Simulation results of the proposed RF-EH version 1.

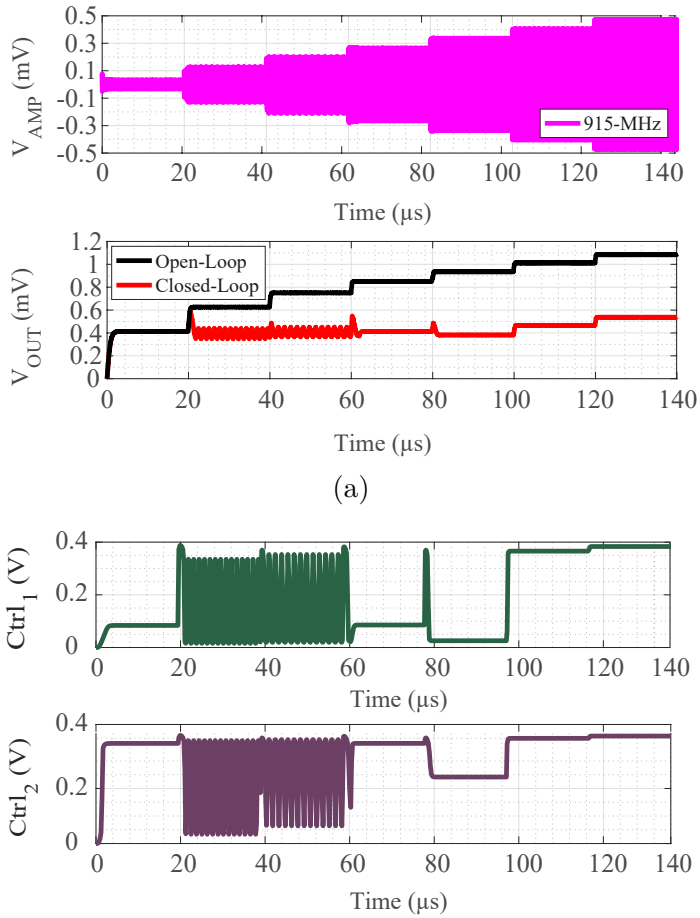
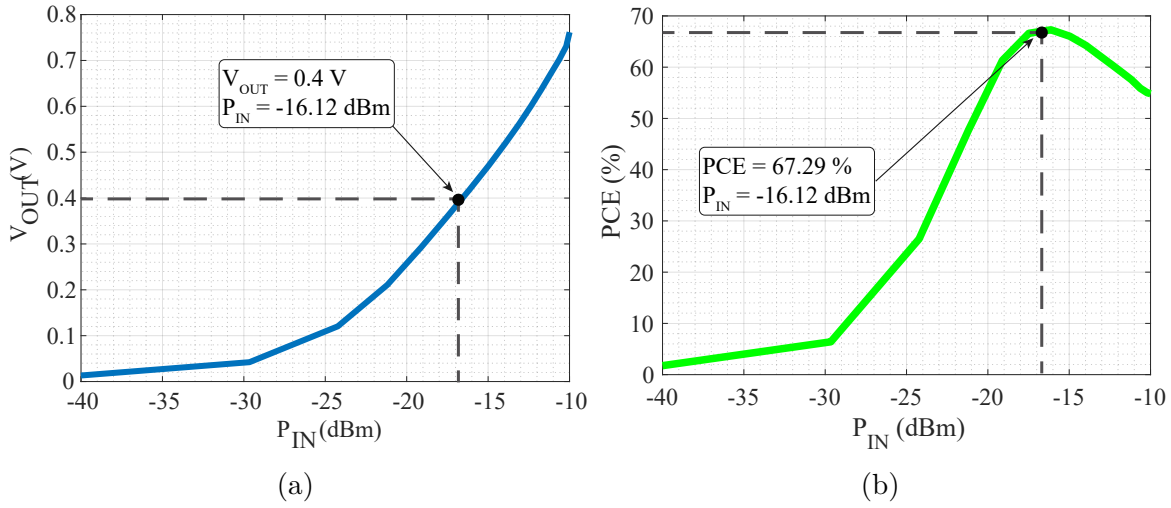


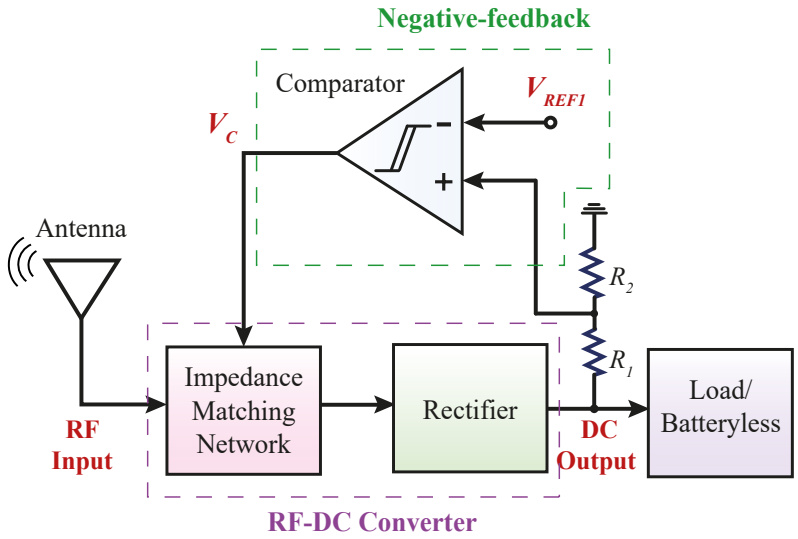
Figure 26 – Analysis of PCE and voltage output according to the RF input power level, for version 1.



4.2 RF-EH VERSION 2 - VARACTOR-BASED

A second version of the RF-EH system based on the adoption of varactors is proposed. The block diagram is depicted in Figure 27, considering the 65-nm CMOS process.

Figure 27 – Varactor-Based block diagram implementation.



4.2.1 RF-DC CONVERTER VERSION 2

Due to the change of the fabrication process from 180 nm to 65 nm, the RF-DC converter had to be resized taking into account this new technology and its new minimum values for the low-V_T transistor previously used. The resizing procedure is discussed in the next subsections, taking into account the same design methodology targeting the maximum value of V_{OUT}.

4.2.1.1 RECTIFIER VERSION 2

The CCDD topology is maintained, and the new transistors channel length and width values are obtained. In the 65 nm process, the minimum L value of the low-V_T transistors is 60 nm and they are initially adopted because of the low parasitic resistance values. The emulated load is kept at 10 kΩ, and the W of the transistors is obtained by parametric analysis of W_p/W_L to achieve the maximum output voltage of the circuit.

After making this variation, it is observed that the circuit saturates at values much lower than the specified 0.4 V, which is due to the reverse short-channel effect. There is a significant increase in V_T in ULV operation, which alters the transistor behavior. To get around this, a fine adjustment is made to the L values. To do this, a parametric analysis of the channel length is carried out. This analysis reveals the need to use a value other than the minimum in this process. Thus, the new value of L adopted in this version is $L_p = L_n = 100$ nm. A new W_p/W_L analysis was carried out, considering the new value

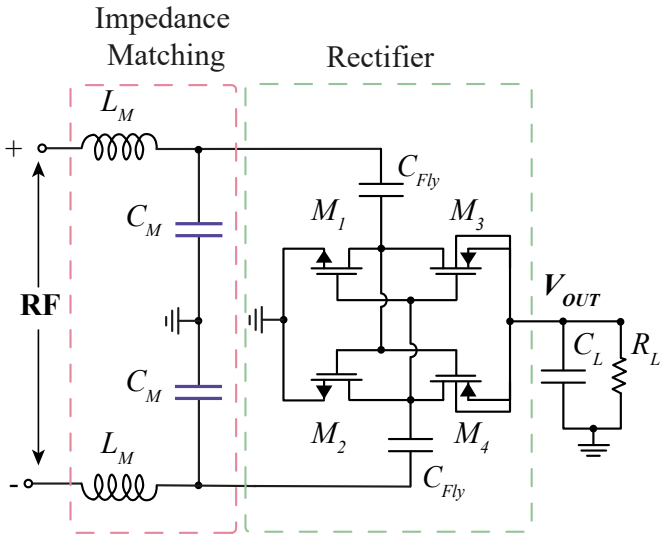
of L, obtaining $W_p = 6.18$ μm and $W_n = 1$ μm, with 14 fingers. The analysis of the flying capacitor is also redone, but there is no change in the value previously adopted, so C_{Fly} remains 5 pF.

4.2.1.2 RECTIFIER INPUT-IMPEDANCE VERSION 2

Based on the new rectifier sizing, the rectifier input-impedance $Z_{RECT} = R_{RECT} + jX_{RECT}$ is also analyzed using the HB technique, obtaining $R_{RECT} = 289.4$ Ω and $C_{RECT} = 190$ fF.

4.2.1.3 IMPEDANCE MATCHING NETWORK VERSION 2

Figure 28 – Impedance Matching Network implementation.



The same consideration as above is adopted, emulating the antenna from a PORT source of $Z_0 = 50$ Ohms. It was observed that $Z_{RECT} \neq Z_0$, where it does not guarantee MPPT and impedance matching is performed. Using the Smith chart technique, the L-C network is obtained with the following values $L_M = 69$ nH and $C_M = 243$ fF.

At first, L_M is considered to be completely off-chip, since the obtained inductance is too high to be integrated with the used CMOS process. Therefore, a more refined analysis was made, considering the inductance of the bond wire which is estimated to be around 4 nH. A new IMN analysis was performed, considering $L_M = L_{EXT} + L_{BW}$, in which L_{EXT} is the of external inductance and L_{BW} is the bond wire inductance. The capacitance of the bond PAD for the target technology is considered as $C_{PAD} = 30.10$ fF, as shown in Figure 28. In this new analysis, the minimum capacitance value of the IMN is equivalent to $C_M = 212.9$ fF.

Figure 29 – Variation of the DC output voltage as a function of the matching capacitor.

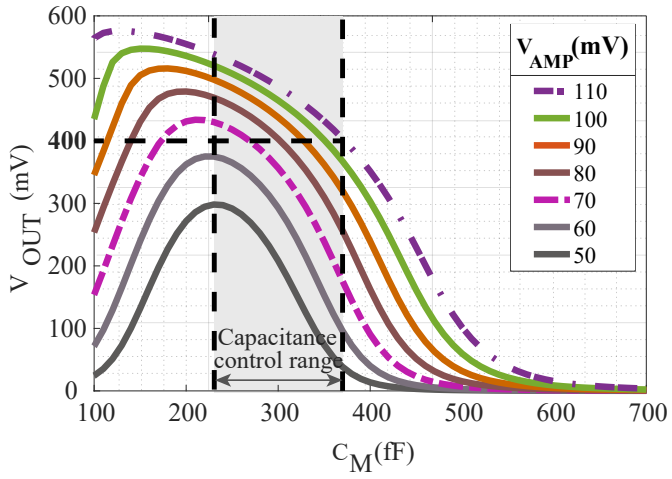
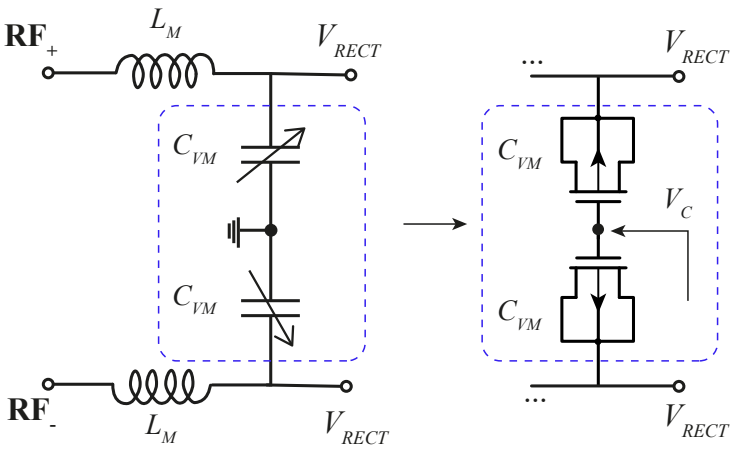


Figure 30 – Composition of the varactors schematic.

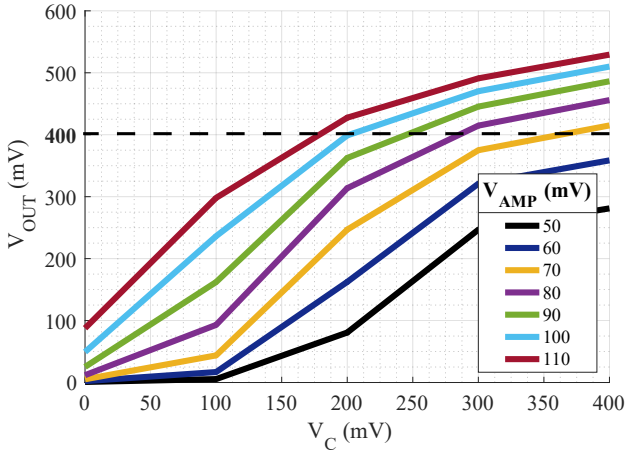


4.2.1.4 ADAPTIVE IMPEDANCE MATCHING VERSION 2

The same analysis was made of the range of values in which the matching capacitor, present in Figure 29, can be varied. The new implementation methodology is made using two varactors (C_{VM}) connected in series, as shown in Figure 30. As one of the objectives is also to reduce the layout area, it can be seen that the implementation of varactors fulfills this condition when compared to the use of switched MiM capacitor banks.

To implement the new control technique, the DC voltage that can be applied to the common terminal of the varactors is considered. Therefore, the varactors are sized with $W = 2.5$ μm and $L = 1$ μm (per finger), and 3 fingers per group and 3 numbers per group to obtain the desired capacitance range when V_C varies from 0 V to 0.4 V. Consequently, the output voltage of the RF-EH can be controlled by the voltage level V_C, as illustrated in Figure 31. Through this analysis, it can be seen that the varactors fulfill the requirement of operating in the desired capacitance range and achieving the desired output voltage value.

Figure 31 – Analysis of the possible control range to be adopted from the output voltage V_{OUT}.



4.2.2 CLOSED-LOOP VOLTAGE REGULATION VERSION 2

The implementation of the closed loop system is based on a negative feedback system, in which an error amplifier is used to control the varactor voltage in order to maintain the DC output voltage (V_{OUT}) at the desired value.

A comparator with a pseudo-differential amplifier topology was adopted with a reference voltage of 0.2 V (external). Only one comparator is enough in this design.

A MOS-varactor was implemented with a continuous variable capacitor. The control logic is implemented by comparing the voltage coming from the rectifier. The output node of the comparator amplifier is connected to the varactors control terminal (V_C) in order to adjust the value of the MOS-varactor C_{VM}.

The proposed RF-EH is optimized to exhibit maximum power transfer at lower input power levels. The output voltage regulation is based on impedance mismatch, causing the excess input power to be converted into reflection at the input when it is higher than that required by the load. And the complete system using the first proposed negative feedback methodology and 65-nm CMOS process is shown in Figure 32.

The V_{OUT} level is measured by employing the resistive divider composed of R_1 and R_2, equal to 100 kΩ. The comparator was implemented using the pseudo-differential amplifier topology, which operates with a supply voltage of 0.4 V. Its reference voltage was adopted as half the voltage value of the power supply ($V_{REF} = 0.2$ V).

Figure 33 shows the results of the complete system simulation when the input RF signal has amplitudes of 35 mV, 70 mV, 105 mV, 140 mV, 175 mV, 210 mV, 245 mV, and an output charge of 10 kΩ. In Fig. 33 it is possible to see the input RF signal and the output regulated and unregulated DC voltage, for the load resistance value adopted.

The output voltage was set to the target voltage level of 0.4 V, and it can be seen that the regulator circuit works from 70 mV of input voltage. The regulation time after the transition is less than 30 μs.

Figure 32 – Complete ULV RF-EH system proposed with varactor-based adaptive IMN.

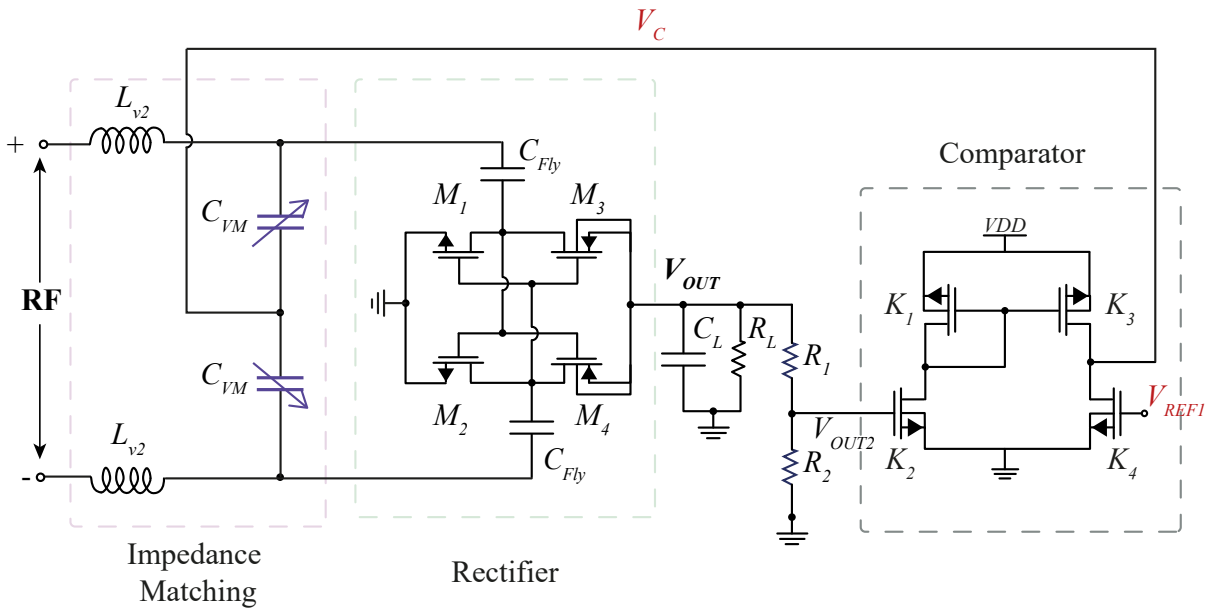
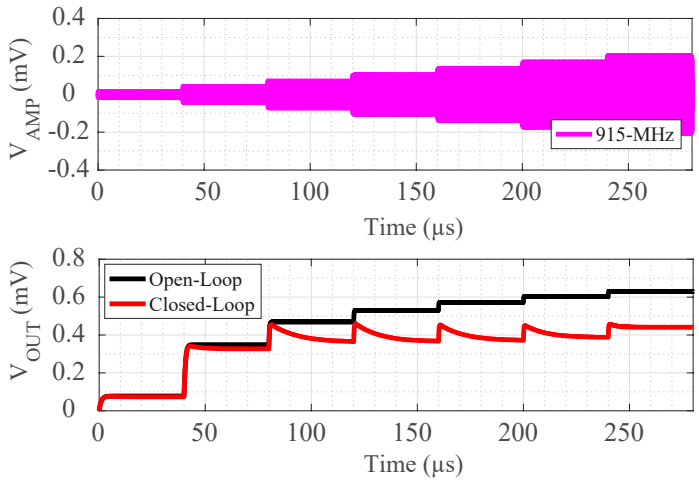


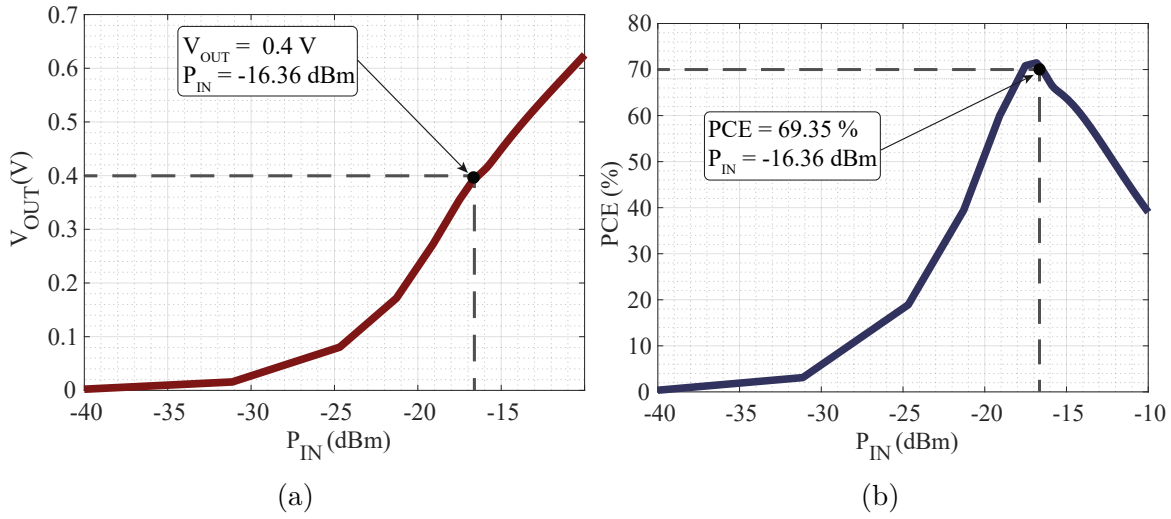
Figure 33 – Simulation results of the proposed RF-EH version 2.



The analysis of PCE and output voltage as a function of input power for this version can be seen in Figures 34b and 34a. It can be seen that the maximum PCE is obtained at the power level where the output voltage reaches 0.4 V. This characteristic was expected since the input match was optimized for that level. The sensitivity of the proposed system can be defined as the minimum power level required to obtain the 0.4 V level at the output. The sensitivity of the proposed system reached a level of -16.36 dBm.

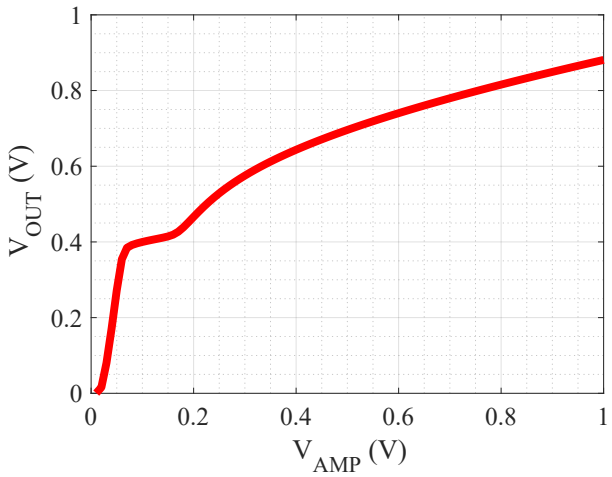
However, after carrying out the PCE and sensitivity measurements that validate the MOS-Varactor version, the competence of this version to keep the RF signal regulated over a wide range was observed. Figure 35 shows that this range occurs over a small variation in the amplitude of the RF signal and can be justified by the fact that the varactor device available in the process used has a small capacitance variation range.

Figure 34 – Analysis of energy conversion efficiency and voltage output according to the RF input power level, for version 2.



(a) (b)

Figure 35 – Analysis of voltage output according to the RF input voltage with the regulation region for version 2.



4.3 RF-EH VERSION 3 - SHUNT TRANSISTOR

Since the nature of the RF signal is to have a wide range of variation, version 3 is proposed with the aim of improving the voltage regulation range of the RF-EH.

Since the RF-EH proposed in this work aims to improve its performance, it is proposed to use transistors in parallel with impedance matching, which aims to be a path for the current to dissipate when the input power is higher, where it can be illustrated in the figure 36.

Figure 37 shows the implementation of shunt transistors, considering the first phase of RF energy harvesting, and its operating principle. It can be seen that when the RF-EH system is collecting higher values of input power from the RF signal, the system will regulate by comparison the value of the output voltage (V_C) that activates the gate of the transistor so that it is a path for current dissipation. When the system is collecting low

values of input power from the RF signal, this regulation system is no longer so necessary, making only the impedance matching optimal and effective.

4.3.1 CLOSED-LOOP VOLTAGE REGULATION VERSION 3

The gate of transistors (T_1 and T_2) is controlled by the feedback signal (V_c), in the same way as the MOS varactor-based topology.

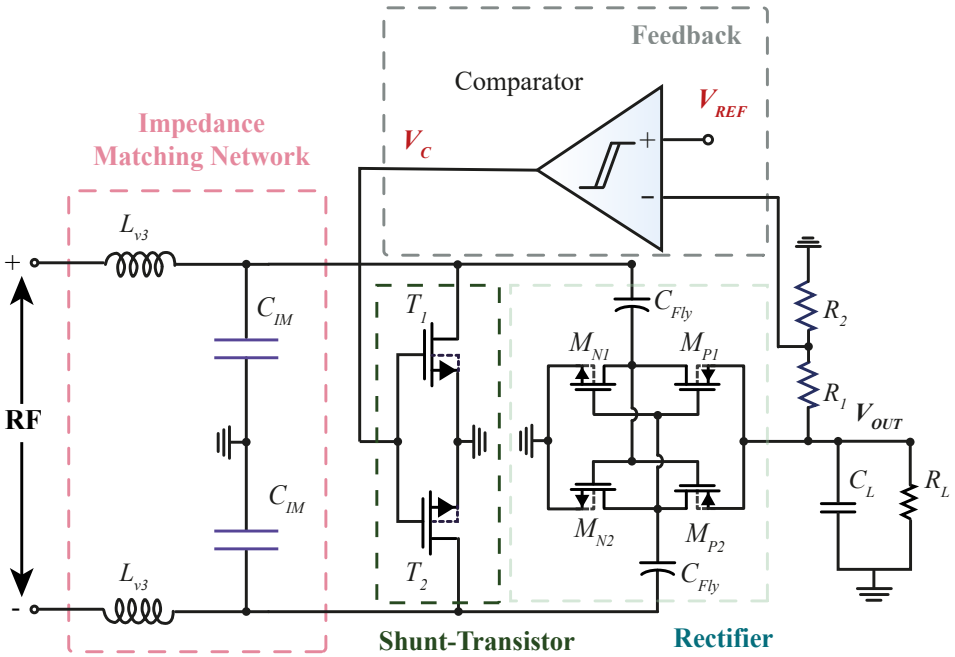
V_c should be equal to 0 V for reduced input power levels in order to avoid affecting impedance matching. Moreover, at higher input power levels, the excess energy can be drained by these transistors, according to the V_c voltage, to keep the output level at 0.4 V. The load values considered are R_L =10 kΩ and C_L = 100 pF.

To carry out the regulation, an OTA with a second stage and an ideal reference voltage of V_{REF} = 0.24 V is adopted, which will be further detailed in Chapter 5. To do this, the resistive divider inserted in the rectifier output had to be set to R_1 = 134 kΩ and R_2 = 200 kΩ.

The PCE and sensitivity of this version can be seen in Figures 38a and 38b, considering that when V_{OUT} = 0.4 V the sensitivity is P_{IN} = -16.13 dBm, so the PCE for this sensitivity is PCE = 62.65 %.

As expected in this version of the RF-EH system, it can be seen from the figure 39 that the output voltage remains regulated over a wide range of RF signal amplitude variations.

Figure 36 – Complete ULV RF-EH system with transistor gate.

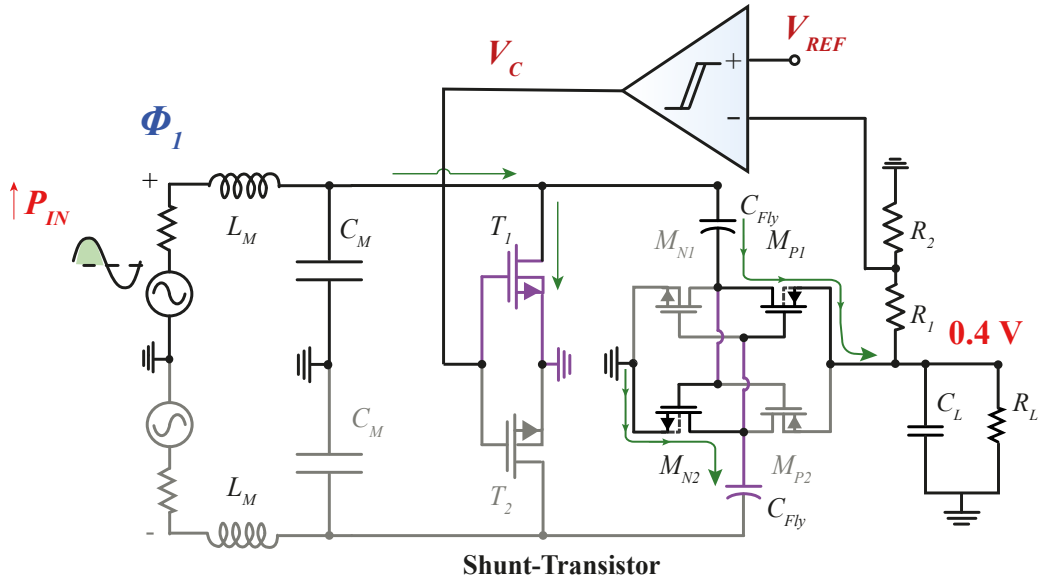


4.4 CONCLUSION OF THIS CHAPTER

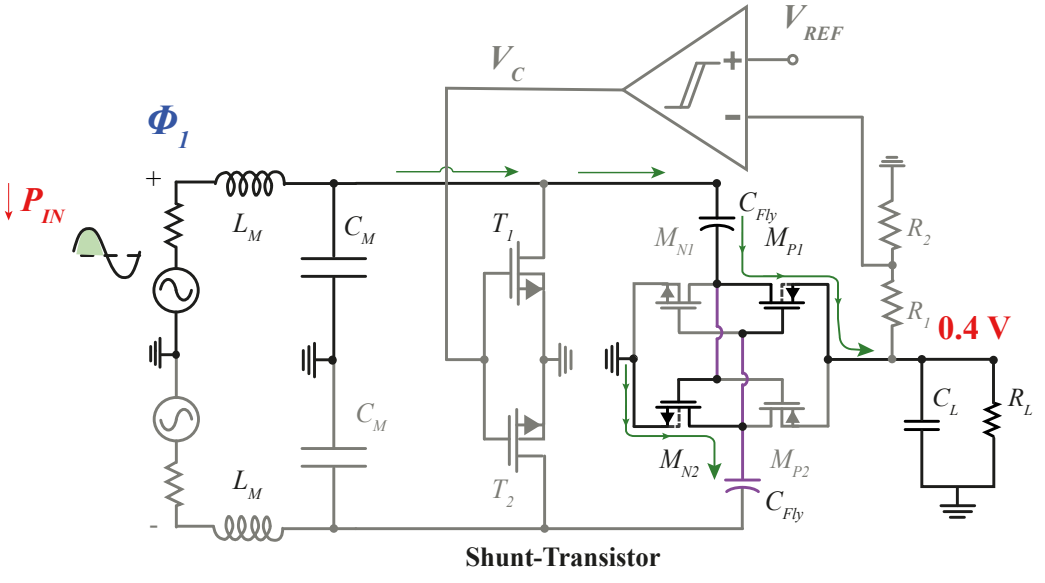
This chapter proposed and presented three versions of the implementation of the self-regulating RF-EH system in a closed-loop voltage regulation based on the impedance control, with an optimization technique for maximum power transfer at low input power levels, in order to ensure the conversion of an ultra-low power input signal, as can be seen in Figure 40.

The version 1 of a system based on a mixed digital-analog and RF circuit was presented, using the 180 nm CMOS process, which obtained a sensitivity of P_{IN} = -16.12

Figure 37 – Shunt-transistor operating principle: 37a - high input power, 37b - low input power.

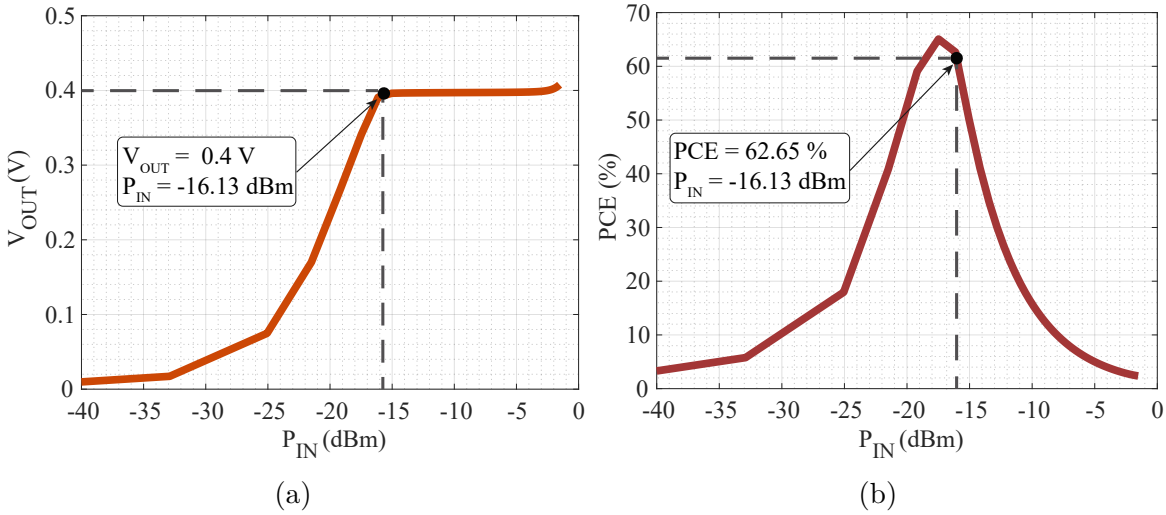


(a)



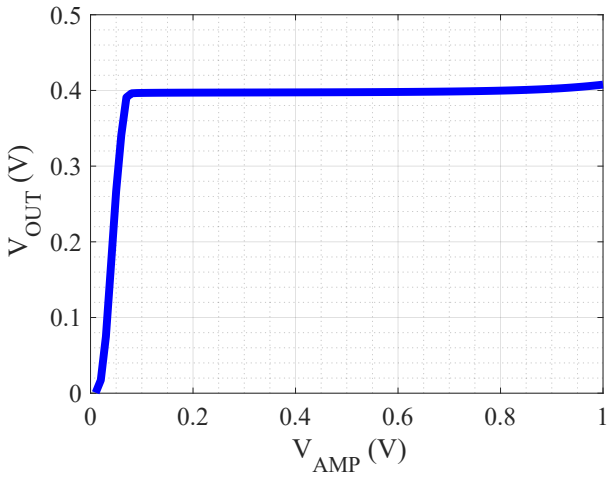
(b)

Figure 38 – Analysis of energy conversion efficiency and voltage output according to the RF input power level, for version 3.



(a) (b)

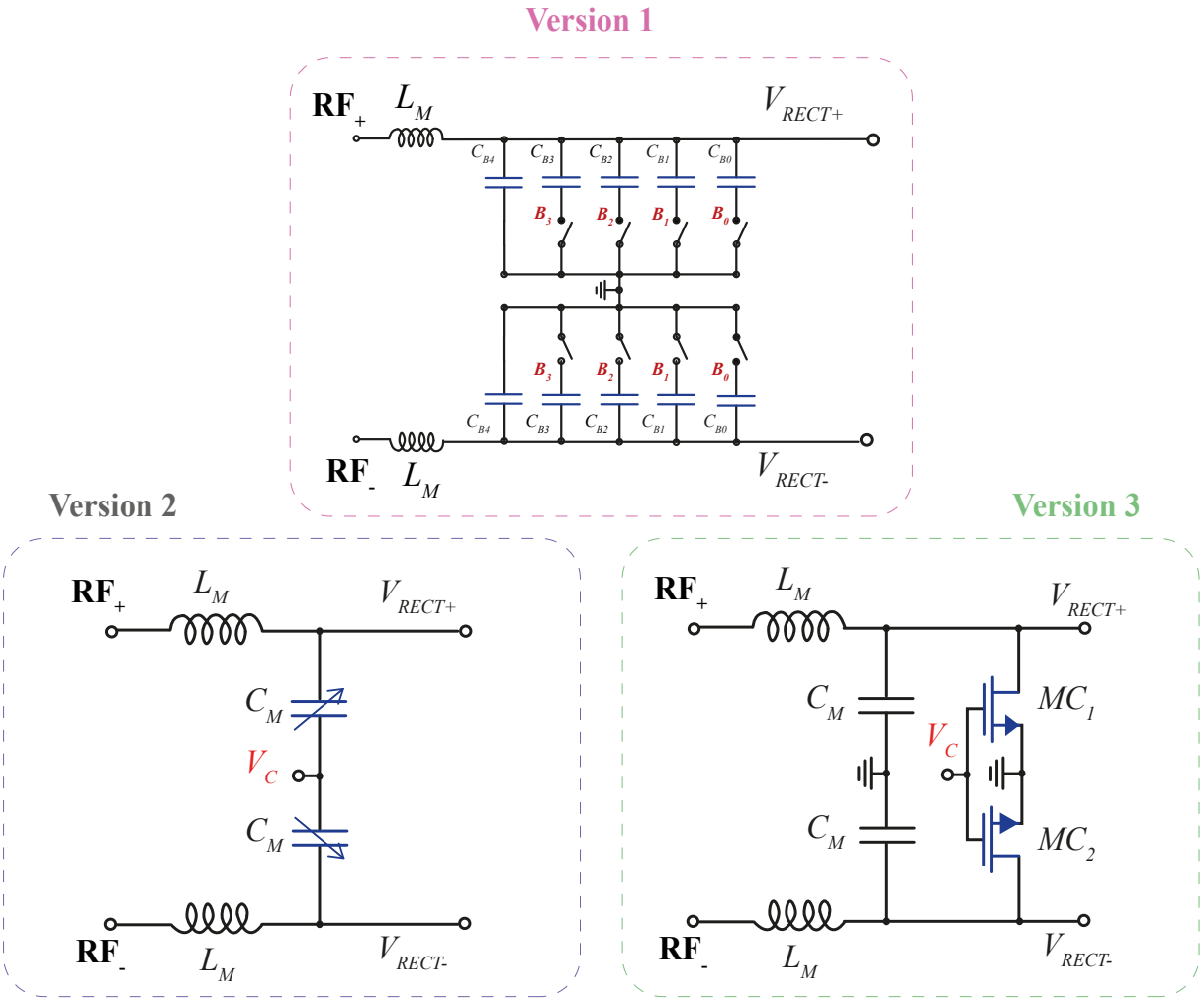
Figure 39 – Analysis of voltage output according to the RF input voltage.



dBm when the output voltage reaches the expected 0.4 V. For this sensitivity, a PCE of 67.29 % was measured. In this system, voltage regulation can be observed for an RF signal amplitude variation of 70 mV to 490 mV. Ideally, this system should have an V_{REF} of 0.2 V and V_{DD} of 0.4 V. It should also be noted that the proposed system had some implementation difficulties, the capacitive bank, for example, had to be readjusted using ideal switches. Furthermore, in order to implement the clock signal generator, it would be necessary to design an oscillator circuit. This oscillator can present significant power dissipation, reducing the effective PCE that can be obtained in the complete circuit implementation.

In addition, the 180 nm process stopped being supplied to universities, making it necessary to migrate technology during the design. After changing technology, a new Z_{RECT} was obtained and also a new analysis of the capacitance variation as a function V_{OUT}, as shown in version 2. In addition, an attempt was made to simplify the system so that it would occupy a smaller implementation area.

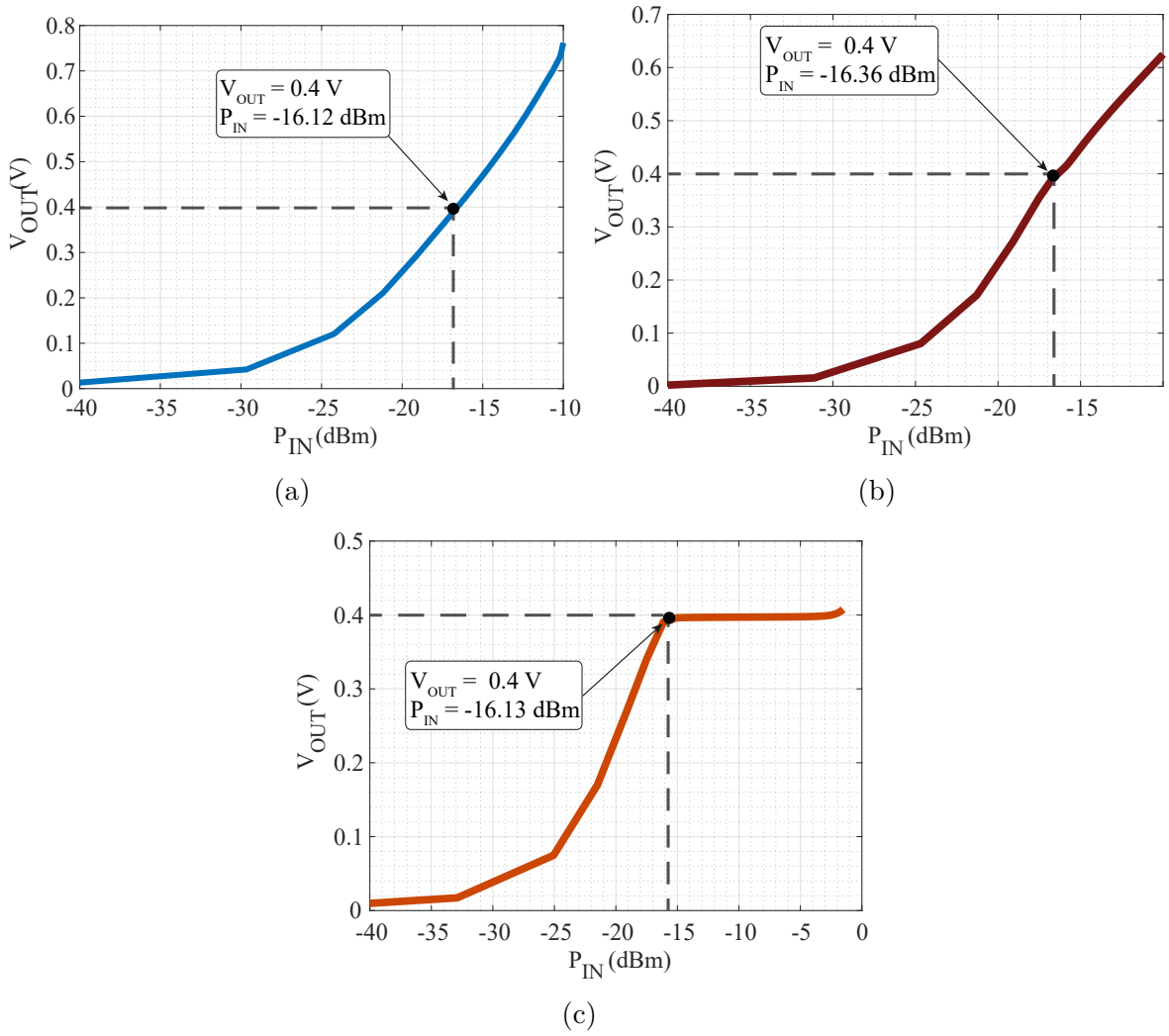
Figure 40 – Versions of the self-regulating RF-EH.



Next, the varactor-mos-based system was implemented, obtaining a sensitivity of -16.36 dBm and a PCE of 69.35 %. In this version the expected result was obtained, considering a simpler system than version 1, however, the regulation range is small, i.e. considering a real case, where the RF signal is variable, the input power can increase, it can no longer act and regulate. Therefore, version 3 of the RF-EH system was proposed and implemented using shunt transistors, with the purpose of regulation when the system is fully matched for low input powers. Considering the variation of the RF signal, the shunt transistors are only activated when the power rises to the desired level, making it a way for a current discharging path. Finally, in version 3 the sensibility is P_{IN} = -16.13 dBm and the PCE = 62.65 %.

Figures 41 and 42 show a comparison of the performance of the three versions of the RF-EH system for voltage regulation based on impedance matching. All versions had their sensitivity obtained when the output voltage was fixed at 0.4 V, and the maximum PCE was extracted from this sensitivity value. In all three versions, the sensitivity is close to -16 dBm, and the best PCE performance is observed in the second version.

Figure 41 – Analysis of the RF signal input power as a function of the 0.4 V output voltage for the three versions presented.



A comparison of regulation performance between the second and third versions is made in Figure 43. There is a trade-off between PCE and input voltage range. Despite the second version having better PCE performance, the third version keeps the system regulated over a wide range of the collected RF signal variation.

Table 6 shows the three versions, considering the design specifications, frequency, output voltage, low RF signal input power, V_{DD} and load, as well as the respective sensitivity, PCE and regulated range results. All three versions use only 1 rectification stage, and all three versions considered the sensitivity and PCE measurements for the complete RF-EH system in a closed loop.

Figure 42 – Power conversion efficiency of the RF-EH for the three versions presented.

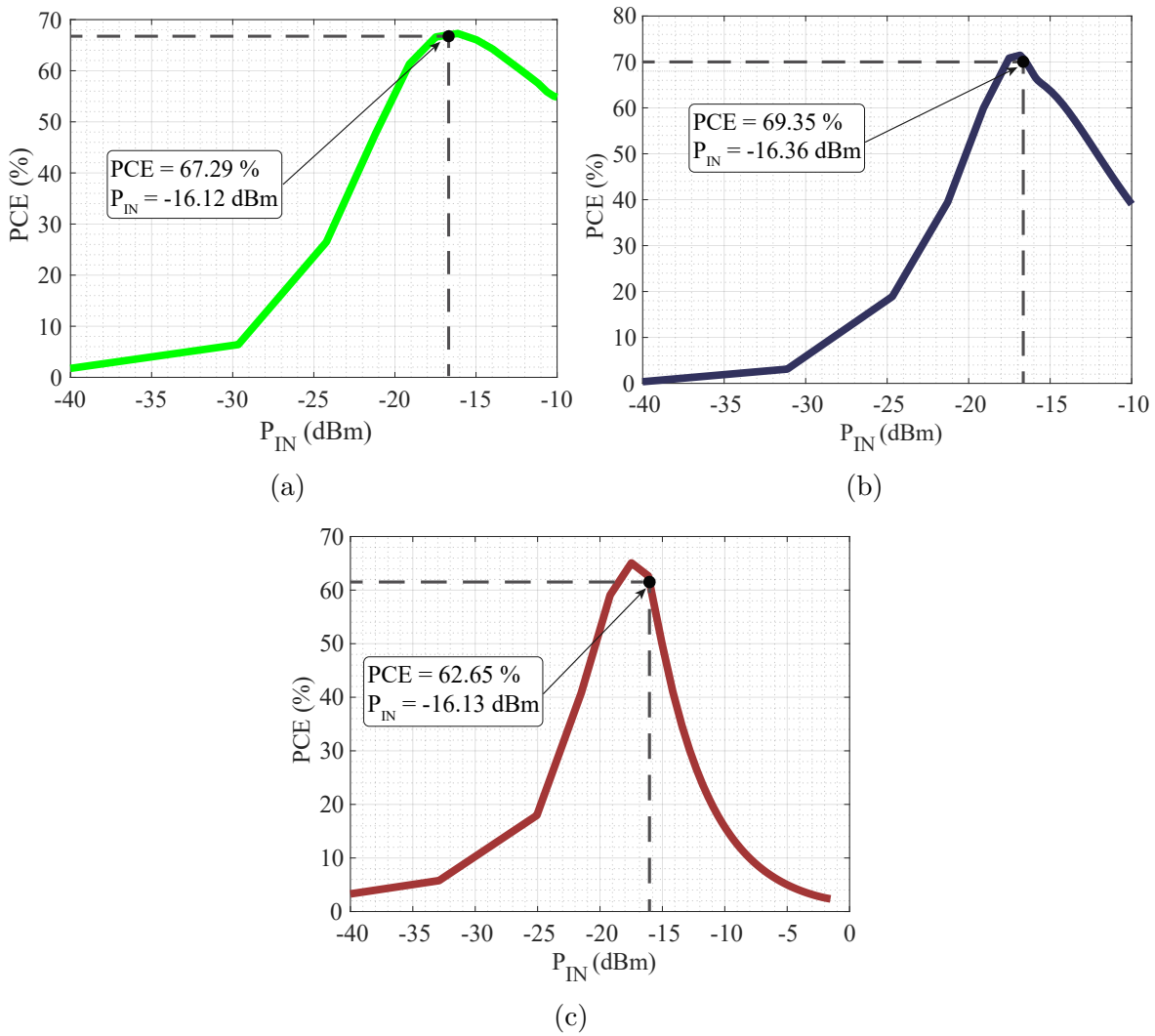


Figure 43 – Analysis of voltage output according to the RF input voltage.

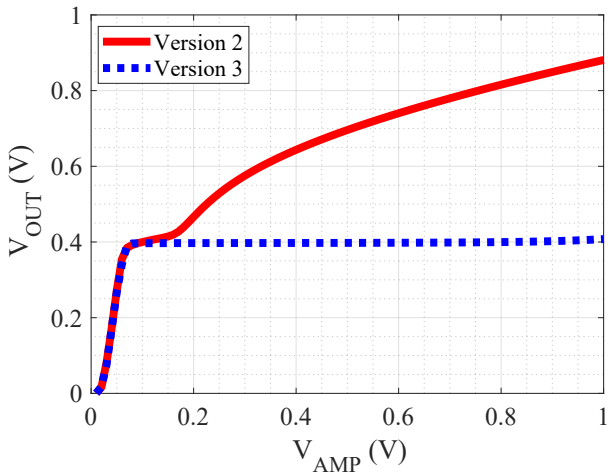


Table 6 – Performance comparison between the three versions of the RF-EH proposed in this work.

Specification	**Version 1**	**Version 2**	**Version 3**
Process (nm)	180	65	65
Freq. (MHz)	915	915	915
Sens. (dBm)	-16.12	-16.36	-16.13
PCE (%)	67.29	69.35	62.65
V_{OUT} (V)	0.4	0.4	0.4
R_L (V)	10	10	10
V_{DD} (V)	0.4	0.4	0.4
N. of stages	1	1	1
Closed-Loop	Yes	Yes	Yes
Reg. Voltage Range (V)	0.07-0.42	0.07-0.17	0.07-1

5 DESIGN OF THE RF-EH AND POST-LAYOUT RESULTS

This chapter presents details on the implementation of shunt-transistor-based voltage regulation in the RF-EH system, as well as the effects of I/O ring capacitances and bond-wire inductance on this design. We analyse the individual results of each block of the system considering parasitic post-layout simulations, and post-layout results of the complete RF-EH.

The complete RF-EH system is shown in Figure 44, which shows the impedance matching technique taking into account the effects of I/O ring capacitances and bond-wire inductance, the cross-coupled rectifier (designed and presented previously in Section 4.2.1) and the output voltage comparison sub-circuit, consisting of the comparator and reference voltage, which make up the closed-loop voltage regulation. The final design of the RF-EH system will be detailed in the following sections.

5.1 IMN CONSIDERING PRACTICAL IMPLEMENTATION ISSUES

As shown in section 4.2, the IMN adopted to satisfy $Z_{RECT} = Z_0$ is based on the passive elements L and C, which make up the L-Network. To allow the circuit fabrication, second-order effects should be considered. The second-order effects in this case are generated by the I/O PADs and ESD parasitic capacitances and the inductance of the bond-wires.

In Figures 45a and 45b we can see how the integrated circuit package after the fabrication of a microchip looks like, where all the circuit layouts and systems that will be considered on this chip are inserted in the die. Around the die, there are ESD protections that aim to prevent electrostatic discharges from occurring (which can occur when a human being touches the device or due to the environment where the circuit is used). Around the protections are inserted the bond PADs, which are nothing more than the pins on which

Figure 44 – Complete ULV RF-EH system proposed in this work.

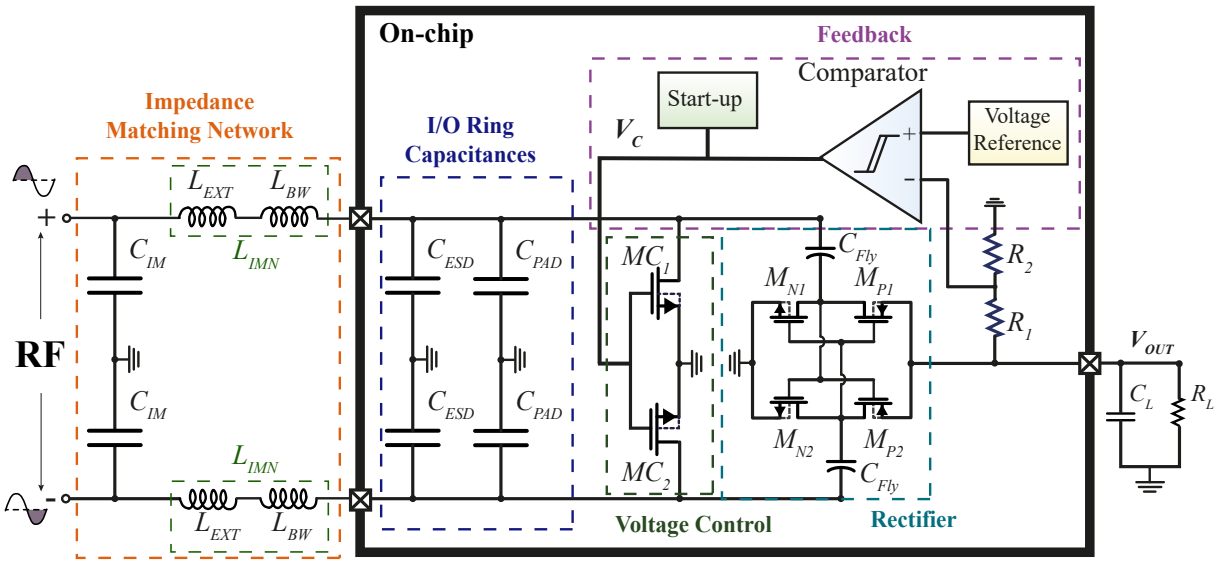
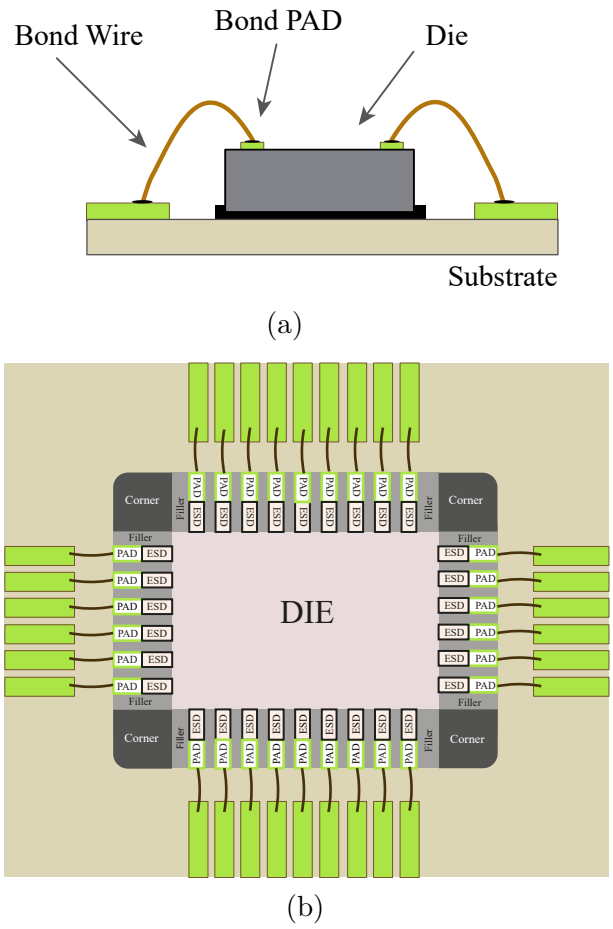
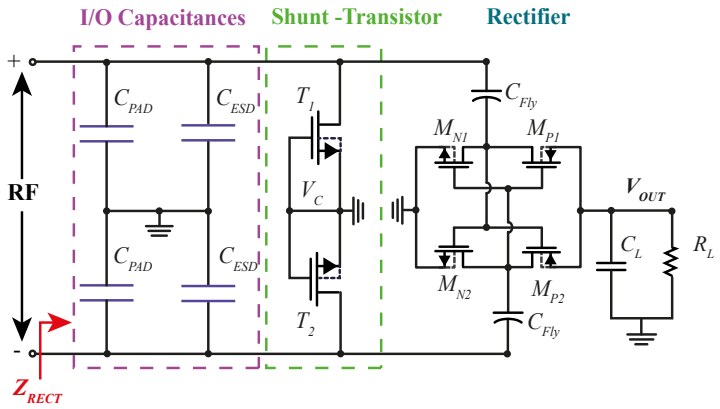


Figure 45 – Representation of the second order effects of a top-level chip. Where 45a is side view, and 45b is top view.



the inputs and outputs, V_{DD}s and V_{SS}s of the subsystems are connected (at this point, the electrical validation test tips are connected). Finally, on all the external bond PADs there are bond-wires connected, which interconnect the microchip with other electronic devices.

Figure 46 – Schematic representation of the second-order effects of I/O ring parasitic capacitances.



The main effects that appear at a higher level and that can affect an RF system are the capacitances and inductances that the ESD, the bonding PADs and the bonding

wires physically have. This is because the IMN is the most sensitive system in the RF design, where any change in capacitance or inductance can totally change the expected result. Therefore, from this point on and to ensure that the RF-EH designed in this work has the best possible performance, these effects are considered at schematic level (Figure 46), so that they can be predicted and fixed in the IMN so that they do not affect the RF-EH.

To do this, the analysis of the equivalent impedance Z_{RECT} is performed again, for the RF signal at 915 MHz. Initially at the schematic level considering only the I/O ring capacitances (estimated from the 65 nm PDK doc to present C_{PAD} = 30.10 fF and C_{ESD} = 326 fF). Thus, a new analysis of the harmonic balance (HB) is carried out, and for a V_{AMP} = 268.93 mV, which reaches 0.4 V output, there is a Z_{RECT} = 28.62 - j289.1 Ω. From the obtained impedance, impedance matching is performed using Smith Chart. As can be seen in Figure 47, from this new rectifier input impedance value, the inverted L network is obtained. It is different of what was seen with an ideal way, which resulted in a traditional L network. This change occurs due to the new capacitances that are inserted into the system, which cause a significant impact on impedance in an RF system.

Once the new impedance-matching arrangement has been obtained, we move on to a more robust analysis of the system. At this point, the layouts of the sub-circuits that compose the RF-EH system were drawn up. Figure 48 shows the layout of the rectifier and the shunt transistors. Once the layout has been carried out and the necessary checks have been made, the parasitic capacitances and resistances of these circuits are extracted, which will also be considered from here on in the system design. As parasitic capacitances, i.e. unwanted capacitances, are taken into account, more capacitances are added to the system, which again affects the IMN. Thus, to get around this situation, the IMN analysis must be adjusted, taking into account the post-layout results.

In the post-layout simulation, a new consideration in the system arrangement

Figure 47 – Bond PAD and bond wire implementation.

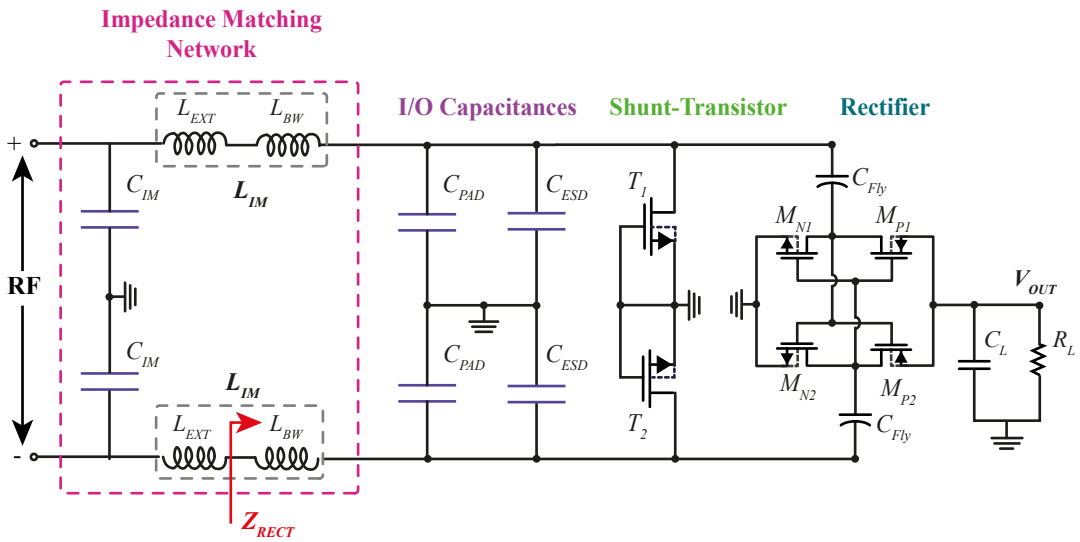
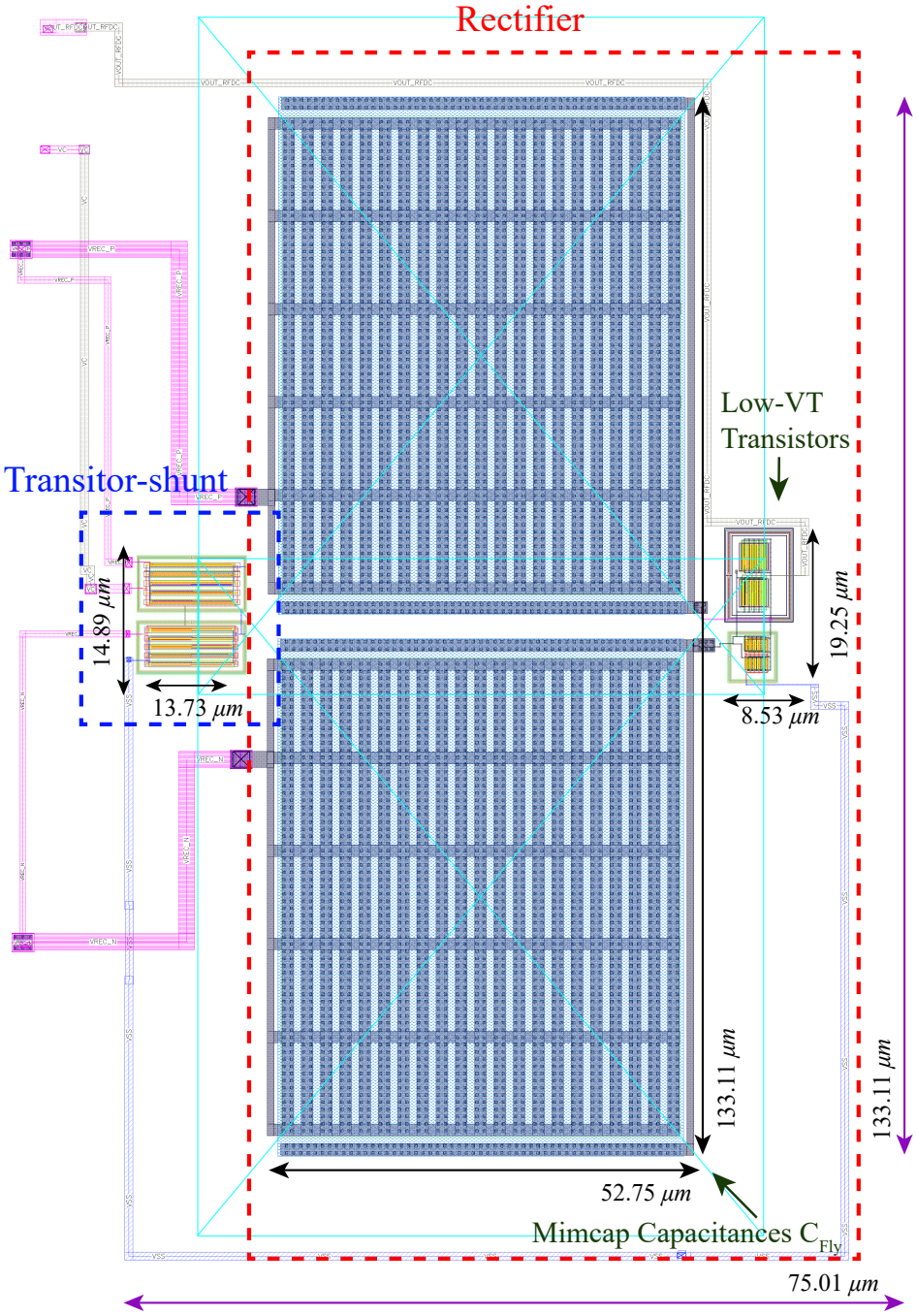


Figure 48 – Layout physical of the rectifier and shunt transistors.



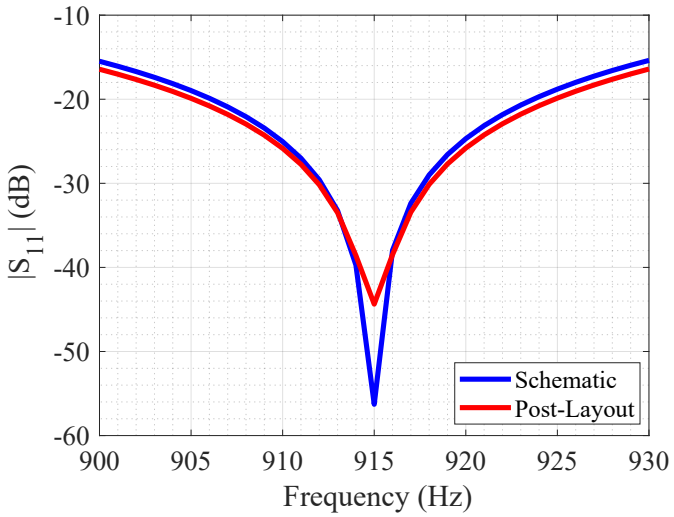
is made, where the bond wire inductance (L_{BW}) is considered equivalent to 4 nH, with quality factor $Q = 14$ according to Michelon et al. (2014).

Therefore, the new IMN, with a value of Z_{RECT} = 24.55 - j217 Ω is obtained by visualizing Z from L_{BW}, as illustrated in Figure 47. The LC arrangement is equivalent to the previous one, with L set to $L_{EXT} = 53.3$ nH and $C_{IMN} = 2.1$ pF.

Post-layout results of $|S_{11}|$ were obtained to validate the impedance matching considering the addition of second-order effects. In this design, the reflection coefficient ($|S_{11}|$) is measured using the load representation of Z_{RECT} obtained previously, where R is

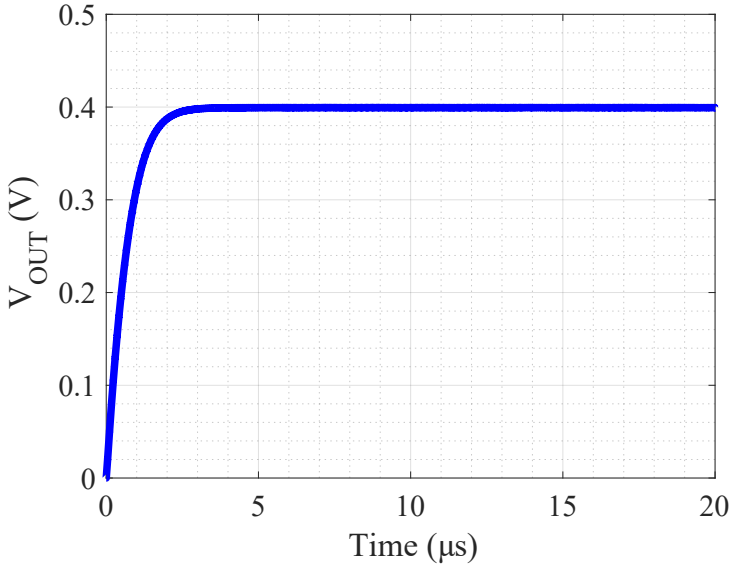
the real impedance and the imaginary part is represented by the reactance of a capacitor $C = \frac{1}{2\pi f X c}$. Figure 49 shows the $|S_{11}|$ for the schematic level, as well as for the post-layout level, where it can be seen that for the schematic there is an $|S_{11}|$ equivalent to -56.28 dB, and for the post-layout $|S_{11}|$ of - 44.36 dB, where both consider the design frequency of 915 MHz.

Figure 49 – Input reflection coefficient $|S_{11}|$ simulation.



The post-layout analysis of the open-loop output voltage as a function of time was carried out, considering the 65-nm process, the RF frequency of 915 MHz and a load of 10 kΩ (Figure 50), where the desired value of V_{OUT} of 0.4 V was obtained, with the minimum input amplitude voltage of 70 mV, after 2.1 μs, with Open Loop PCE of 51.11 % and sensitivity of -16.12 dBm.

Figure 50 – Transient analysis of the RF-EH open-loop output voltage of a input amplitude of 70 mV.



5.2 REGULATION FEEDBACK CIRCUIT

After carrying out the impedance matching considering the adjustments due to the I/O ring capacitances and bondwire inductances, the circuits that make up the RF-EH voltage regulation will be discussed next, as shown in Figure 51.

The resistive divider, reference voltage, comparator and startup circuits were previously presented during this dissertation as a part of the voltage regulation block proposed in this work. Thus their circuit implementation will be detailed in the following subsections, along with their respective layouts and post-layout simulations.

5.2.1 VOLTAGE REFERENCE

As shown in the previous chapter, for the comparator to perform voltage regulation it would be necessary to generate a voltage reference (V_{REF}) of approximately 0.2 V. This value was initially considered to be half of the rectifier output voltage level, to satisfy the control conditions and also to improve the comparator dynamic range.

For this purpose, the two-transistor (2-T) topology represented in Figure 52, is adapted from Seok et al. (2012). It generates voltage references for low-power circuits and avoids amplifiers, saturated devices, or resistors to meet power, area and minimum functional requirements.

Voltage V_{REF} is obtained considering two transistors, called 2-T transistors, Nv_{na} and Nv_{hvt}, where the first one is native-VT and the second one is high-VT, operating in the subthreshold region, to obtain a stable output voltage level, and supply voltage equal to $V_{DD} = 0.4$ V.

Figure 51 – Voltage regulation proposed in this work.

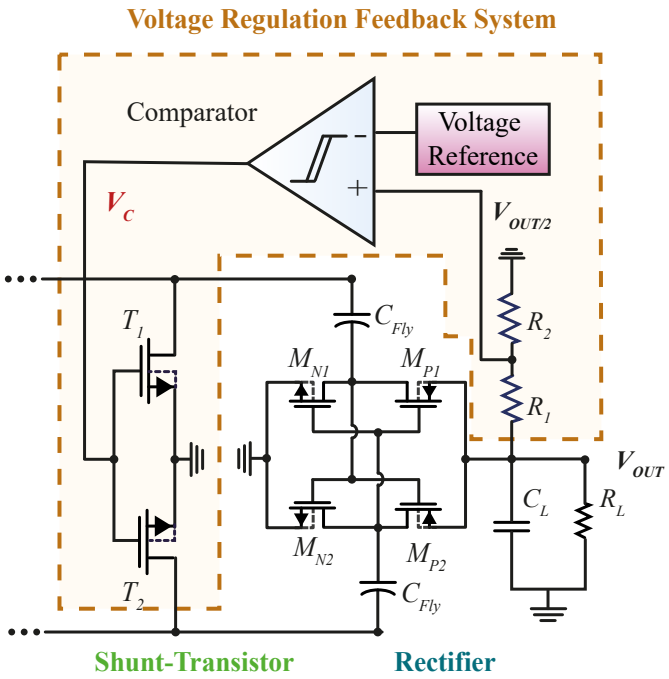
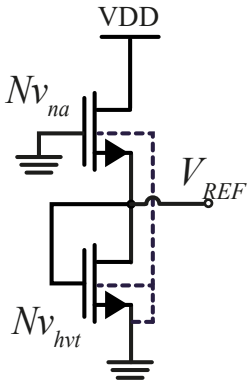


Figure 52 – 2-T voltage reference schematic.



Source: Adapted of Seok et al. (2012).

Figure 53 – Voltage reference (V_{REF}) in function of the supply voltage (V_{DD}).

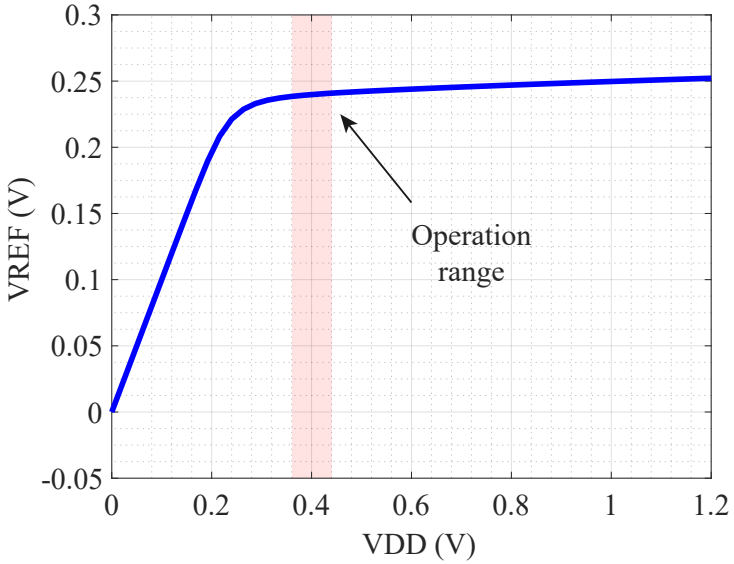
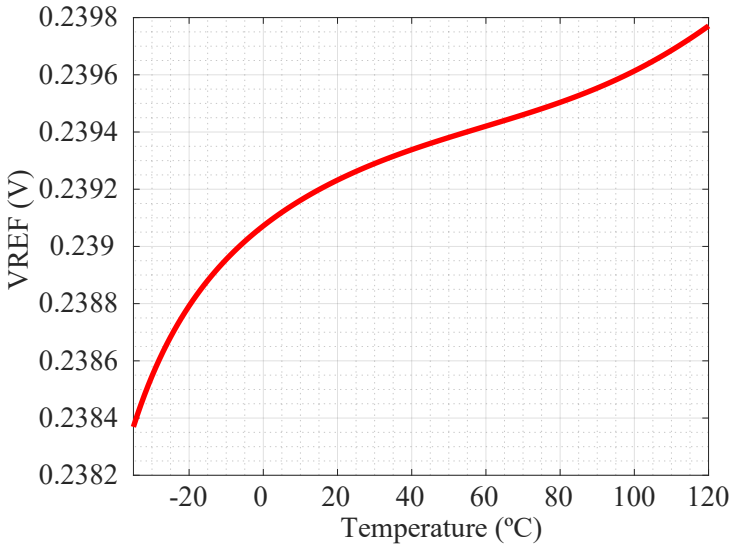


Figure 54 – Voltage reference (V_{REF}) in function of the Temperature (TC).



According to Seok et al. (2012) some considerations have to be made in order to achieve the sizing specification: $VDS_{Nv_{na}}$ and $VDS_{Nv_{hvt}}$ must be $> 5 - 6VT$, where

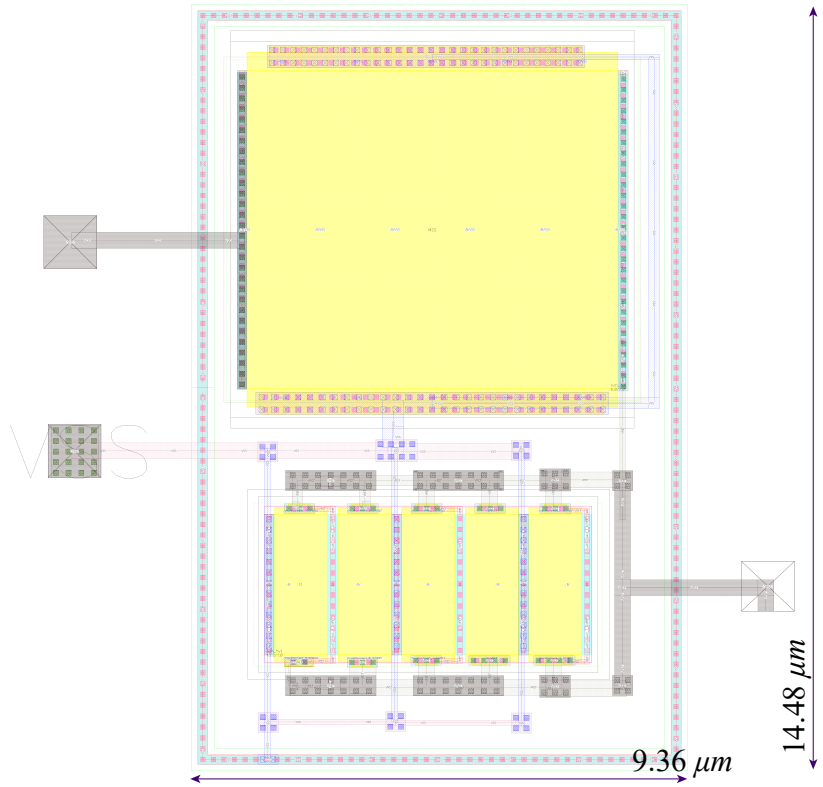
$VT = kt/q$ (approximately 26 mV), and, Nv_{na} follows the subthreshold equation in V_{GS} - V_{REF} considering it the minimum value of V_{GS} that guarantees $< 1\%$ loss of precision, and also considers GIDL (gate-induced drain leakage), where this cannot be significant at the operating point. Therefore, the sizing of V_{REF} is performed and resulted in $Nv_{na} = 6\ \mu$m/7 μm and $Nv_{hvt} = 2.64\ \mu$m/1 μm, with 5 fingers.

Considering this topology, the best voltage reference value that is close to the ideal value of 0.2 V is $V_{REF} = 0.239$ V. Based on this, some analyses were carried out to validate a voltage reference circuit, namely the V_{REF} x VDD analysis (reference voltage as a function of VDD variation) and the V_{REF} x TC analysis (reference voltage as a function of temperature variation).

The V_{REF} x VDD analysis, as shown in Figure 53 it can be concluded that after 0.25 V the V_{REF} begins to stabilize at the design value of 0.4 V, so considering a range of 0.3 V to 0.5 V of V_{DD} , the V_{REF} varies from approximately 0.238 V to 0.239 V.

As for the V_{REF} x TC analysis, as illustrated in Figure 54 it can be concluded that the V_{REF} varied from 0.2384 V to 0.2398 V, with the temperature varying from -40^{o}C to 120^{o}C, resulting in an average rate of 8.75 μV/^{o}C. In addition, the temperature variation when divided by the nominal reference voltage, results in 36.61 ppm/^{o}C.

Figure 55 – Voltage reference layout physical.

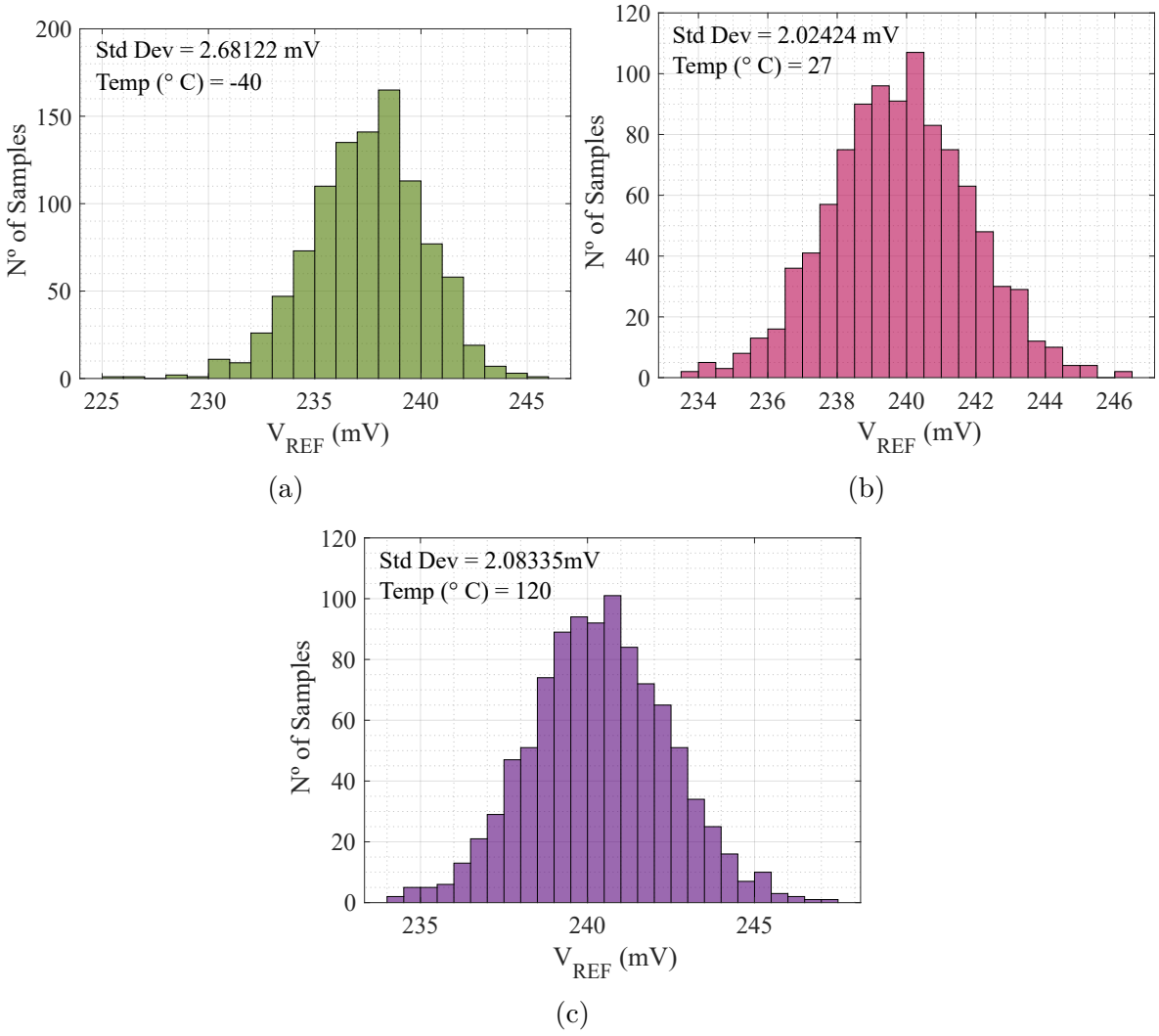


The physical design of this circuit is shown in Figure 55, with a dimension of 9.36 μm x 14.48 μm. This shows the use of core native nmos and core high vt nmos transistors, the latter being designed with 5 fingers. The layout design aimed to maintain

symmetry so that the reference voltage would vary less. In addition, as there are only two NMOS transistors, a PSubGuardring substrate is used for V_{SS}.

Post-layout simulations of V_{REF} were carried out, and from the extraction of the parasites, the variation analysis of the Monte Carlo (MC) process and a corner analysis were carried out, where three temperatures are simulated (-40^{o}C, 27^{o}C and 120^{o}C). The MC results are shown in Figure 56, where for a temperature of -40^{o}C there is a standard deviation (Std Dev) of 2.68122 mV (Figure 56a), for 27^{o}C there is a Std Dev of 2.02424 mV (Figure 56b) and for 120^{o}C there is a Std Dev of 2.08335 mV (Figure 56c). Based on these results, it can be concluded that the topology adopted and the sizing carried out meet the voltage reference requirements for ultra-low voltage and have good performance, with low process variation.

Figure 56 – Power conversion efficiency of the RF-EH for the three versions presented.



5.2.2 RESISTIVE DIVIDER

A resistive divider is considered at the input of the comparator, which is also the output of the rectifier, so from now on in this design V_{IN} will be considered $V_{OUT/2}$, as illustrated in Figure 51.

As seen above during the design of the voltage reference, the value obtained by scaling to ULV was 0.239 V. The comparator non-inverting input needs to be at the same value when the desired output voltage level is reached. To do this, a resistive divider is inserted into the rectifier's V_{OUT} (which should be 0.4 V) and adjusted to 0.239 mV, taking into account Equation 5.1.

$$V_{REF} = \frac{R2}{(R1 + R2)} V_{OUT} \tag{5.1}$$

Here, V_{REF} is the voltage reference value, R_1 and R_2 are the resistors of the voltage divider, and V_{OUT} is the rectifier output voltage.

The physical layout of the resistive divider is made and shown in Figure 57 where resistors of the rppolywo_m type are used, which has the largest resistance per square in the 65 nm process. However, at the layout level, it was noted that fine adjustment is needed to ensure the best performance of the resistive divider, and compromise with the design area, so the resistors were sized at $R_1 = 134$ kΩ and $R_2 = 200$ kΩ respectively. The layout area of the resistive divider is 78.35 μm x 33.96 μm.

5.2.3 COMPARATOR

As seen in chapter 4, the methodology for implementing the closed-loop system with feedback is based on comparing the DC signal with a voltage reference. To this end, a pseudo-differential amplifier operating as a comparator was initially adopted. The use of this topology had been adopted for its optimum performance in ultra-low power applications, but in this design, the pseudo-differential had a low gain, which directly impacted the regulation performance. To get around this, at this stage of the design, the classic two-stage miller-operational transconductance amplifier (OTA) topology was adopted (Figure 58), which in addition to higher gain, also has the advantage of low power consumption and linearity (regulation performance).

The implementation of the reference current for the comparison was considered, for which the same V_{REF} designed previously is used as the basis for generating a stable reference current. A pseudo-differential amplifier is used to make the voltage drop in the R_{2A} resistor result in a voltage equal to V_{REF} at the drain terminal of the M_{1A} transistor. The R_{2A} resistor is implemented outside the chip, due to its size and also so that it is possible to adjust the current level externally.

To design this topology, the comparator is supposed to amplify the difference between two input voltages and suppress any voltage common to the two inputs, as shown

Figure 57 – Physical layout of resistiver divider.

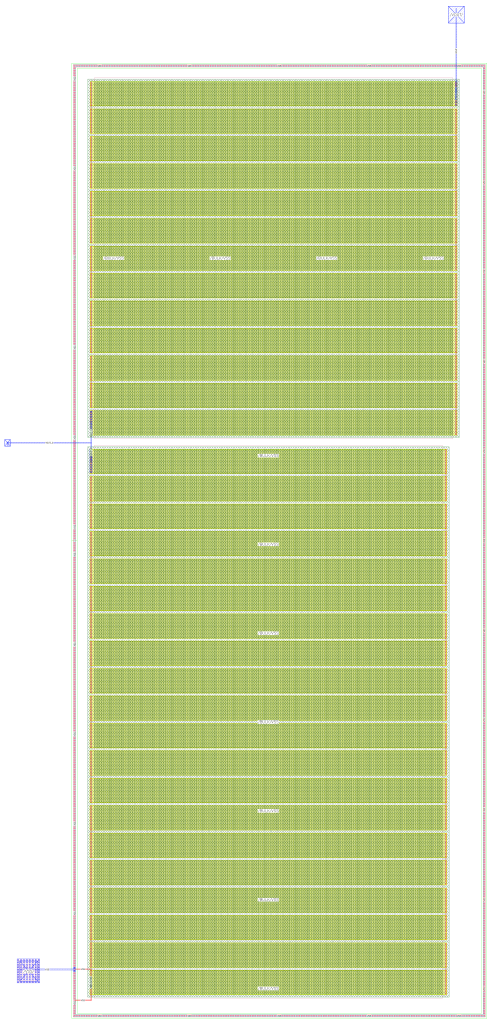
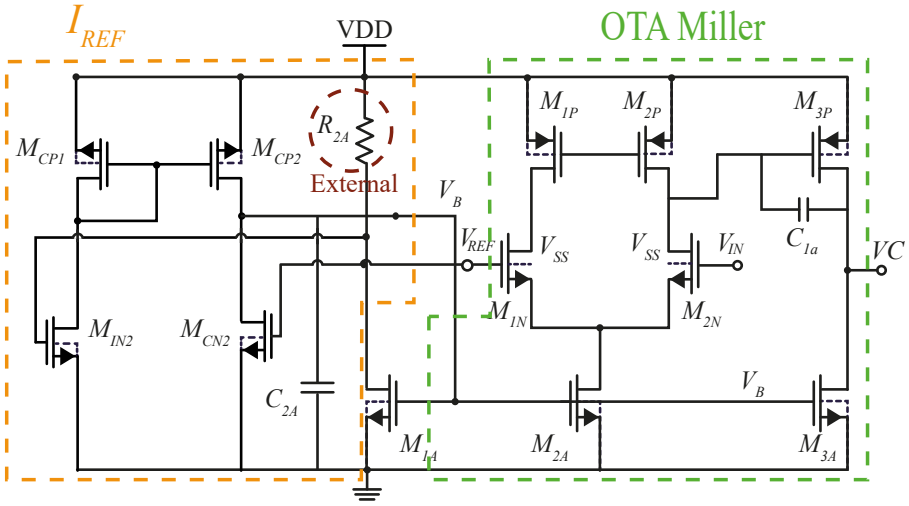


Figure 58 – Classic comparator two-stages with the current reference implementation.



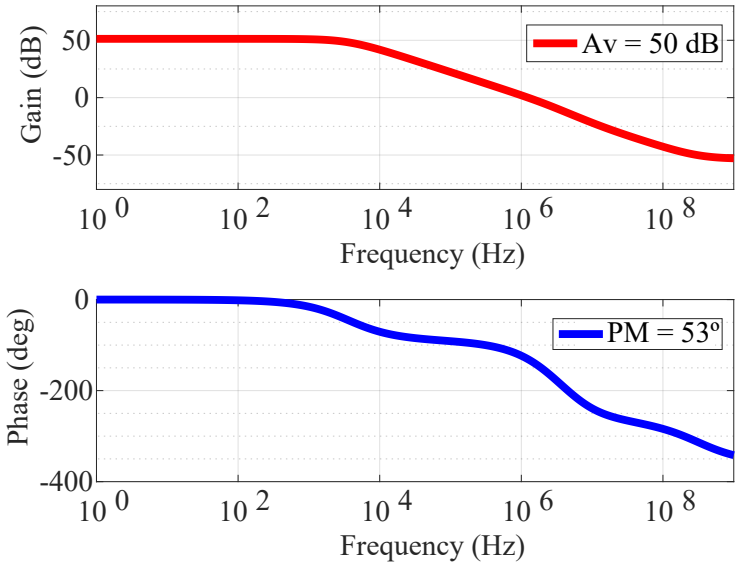
in Equation 5.2.

$$V_C = A\left(\left(\frac{R2}{(R1+R2)}V_{OUT}\right) - V_{REF}\right) \tag{5.2}$$

Here, V_C is the output voltage comparator, V_{OUT} is the output voltage of the rectifier that feed the positive terminal, and V_{REF} is the voltage reference feed the negative comparator terminal.

The voltage output rectifier feeds the positive terminal of the input comparator and the voltage reference feeds the negative terminal of the input comparator. The output voltage of the comparator (V_C) is the voltage control that goes to the gate of the shunt transistors (as illustrated in Figure 51).

Figure 59 – Frequency response analysis of the comparator.



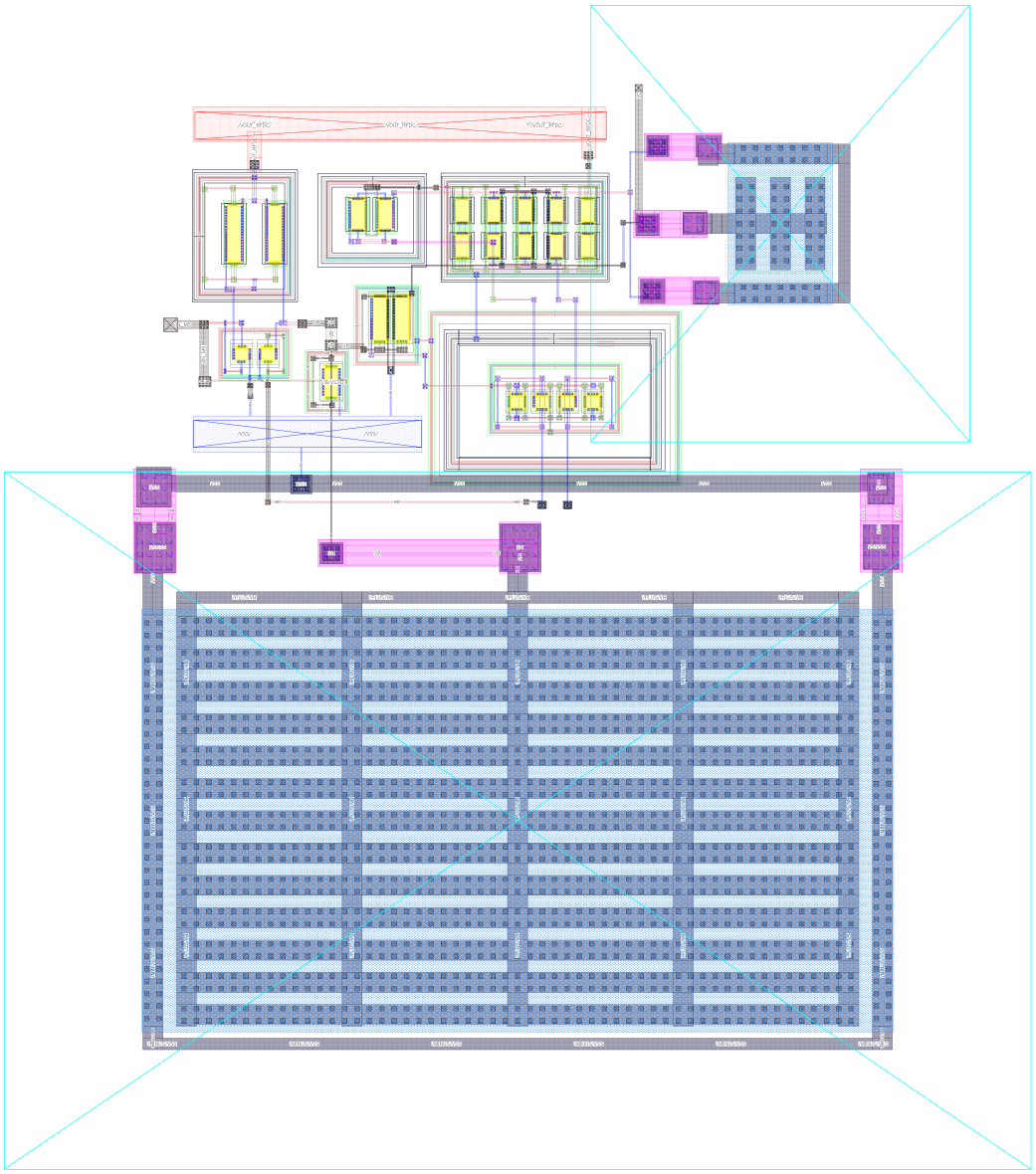
At this stage of the design, all the circuits must be powered by the RF-EH itself and the OTA reference current must be generated internally.

For the design of the comparator, the differential stage is initially designed to find a V_{DS} in the transistors of approximately 0. 2 V. After some adjustments, $M_{1P} = M_{2P} =$ 2 μm/1 μm, with 6 multipliers, and $M_{1N} = M_{2N} = 800$ nm/1 μm. It was later found that it would need a current of $I_S = 70$ nA and for this, a current reference was designed with $M_{1A} = 2$ μm/1 μm and $M_{2A} = 3$ μm/1 μm. This led to the need to increase the gain of this amplifier, so the second stage was designed, where $M_{3P} = 1.5$ μm/1 μm and $M_{3A} =$ 3 μm/1 μm. Finally, pole compensation is considered through a capacitor at the output of the first stage, connected to the V_C output of $C_{1a} = 100$ fF to ensure stability. The power supply for this topology is assumed to be $V_{DD} = 0.4$ V, and comes from the RF-EH itself.

The obtained frequency response can be seen in Figure 59, where we obtained a phase margin of $PM = 53°$, a gain of $Av = 50$ dB and $G_{BW} = 1.2$ MHz. To obtain these results, the gate capacitance of the shunt transistors is taken as the OTA Miller load.

Figure 60 shows the physical layout of the complete comparator, and finally, an analysis of the variation in the input offset is carried out, where post-layout simulations are considered. For this, a transient analysis is carried out with 20 μs, considering $V_{DD} = 0.4$ V, and $V_{IN} = V_{REF} = 0.239$ mV (value obtained previously during the design of the reference

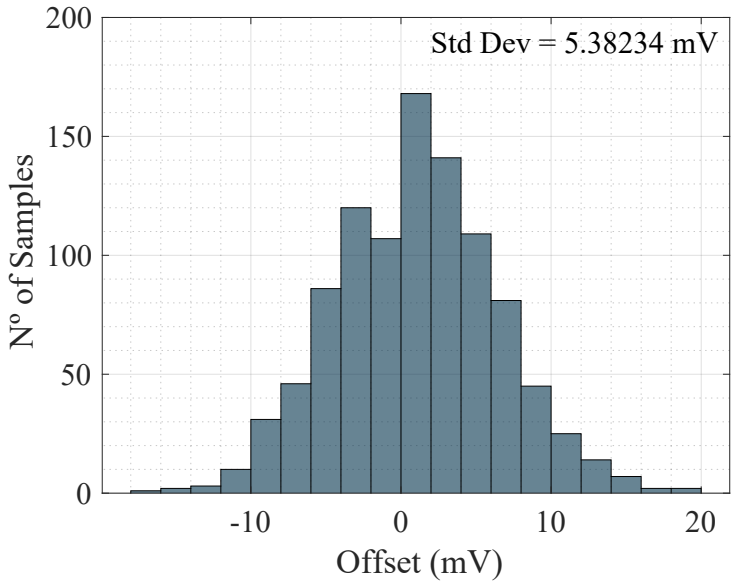
Figure 60 – Physical layout of the comparator.



voltage). The voltage offset is analyzed considering mismatch analysis with 1000 rounds. The results can be seen in Figure 61, where a standard deviation of 5.38234 mV is obtained.

The voltage regulation system was added to the RF-EH, and the output voltage V_{OUT} is now considered to be the V_{DD} of the complete system, thus becoming a self-powered system.

Figure 61 – Mismatch analysis of the offset comparator.



5.3 STARTUP CIRCUIT

Considering a post-layout transient analysis of the output voltage of the self-regulating system, if V_{DD} is different from 0.4 V, the output of the comparator (V_C) could be higher than 0 V, which would cause the shunt transistors to conduct, reducing the rectifier's ability to raise the output voltage level, as can be seen in Figure 62, where in addition, from the result seen in this figure, the circuit could stop operating if this condition is not met. Thus, VC = 0 V is mandatory during the start of system charging and, to satisfy it, a start-up circuit allows the circuit to self-power.

This time is the charging time, and ends up influencing a delay in every system that depends on the 0.4 V of V_{DD}. This delay ends up affecting the control, which is lost during this time because it doesn't have enough voltage to operate. This analysis led to the need to implement a startup circuit.

Figure 62 – Transient analysis of the closed-loop output voltage considering comparator control.

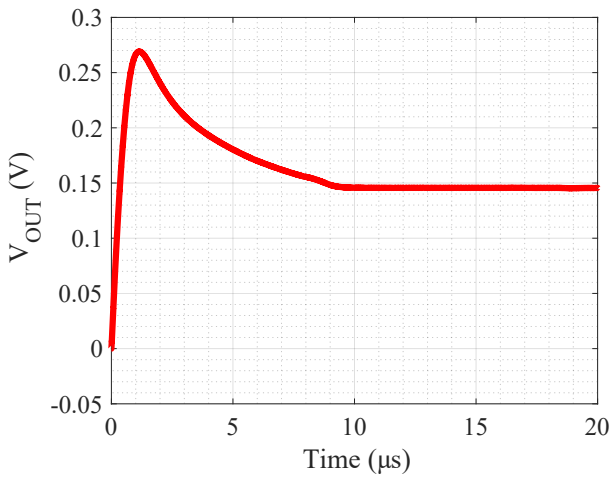
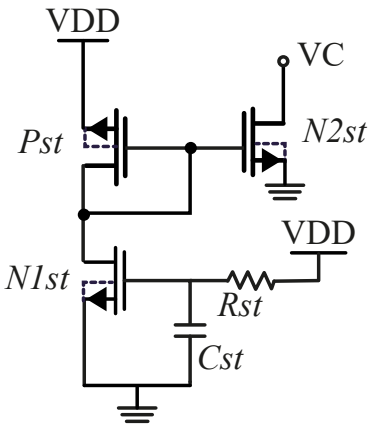


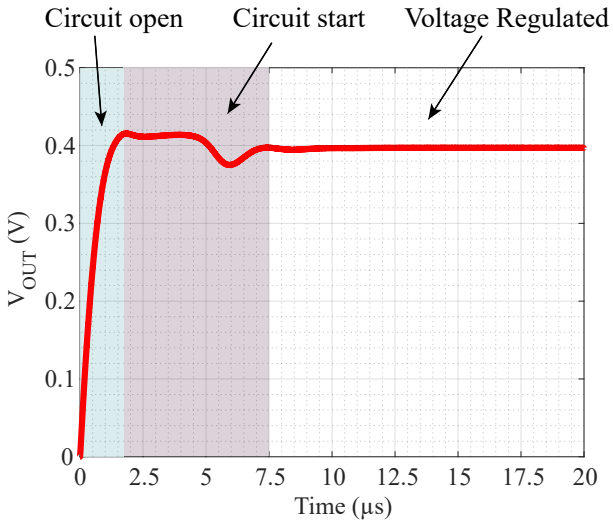
Figure 63 – Startup Schematic.



The proposed startup circuit causes a delay, maintaining the open-loop operation until the output voltage exceeds the value of 0.4 V, properly aligning the reference voltage and the comparator, after which the circuit begins to operate in a closed loop and so does the entire operation.

The startup topology adopted in this work is shown in Figure 63, where the function of the RC filter is to make transistor $N1st$ take longer to conduct, so it makes the gate voltage of $N2st$ equal to V_{DD}, and V_C is forced to V_{SS}. After the time given by RC, $N1st$ conducts, bringing the gate of $N2st$ to zero and thus enabling V_C to be controlled by the comparator.

Figure 64 – Post-layout analysis of the output voltage as a function of the time, with auto-startup.

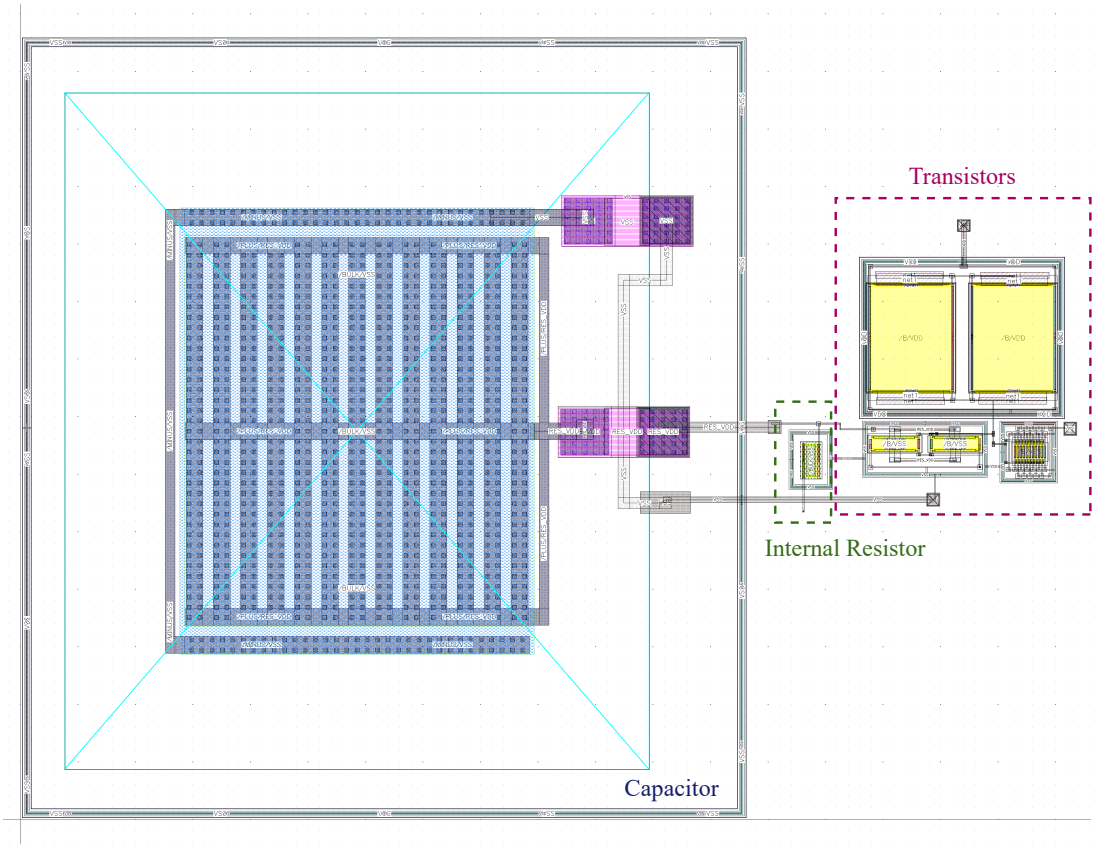


The design of this circuit considers low-VT transistors, where we obtained the dimensions of $Pst = 9\ \mu$m/7 μm with 1 finger and 2 multipliers, $N1st = 800$ nm/4 μm with 1 finger and 2 multipliers, $N2st = 1\ \mu$m/60 nm with 10 fingers to generate the necessary delay in the system. In addition, an R-C low-pass filter is also implemented, where $Cst = 2$ pF and $Rst = 3.2$ MΩ.

The physical layout of the startup circuit is shown in Figure 65. The validation

simulations are then carried out considering the post-layout, as shown in Figure 64 the output voltage, obtaining 0.4 V for different RF signal amplitude levels, where the startup keeps the circuit in open loop until approximately 1. 7 μs, after which the circuit starts operating from 1.7 μs to 7.5 μs, and only after 7.5 μs, the output voltage regulation starts. The input voltage of the RF signal amplitude used in this simulation is 90 mV considering an R_L load of 10 kΩ. Finally, *Rst* is considered external to allow testing of the startup circuit.

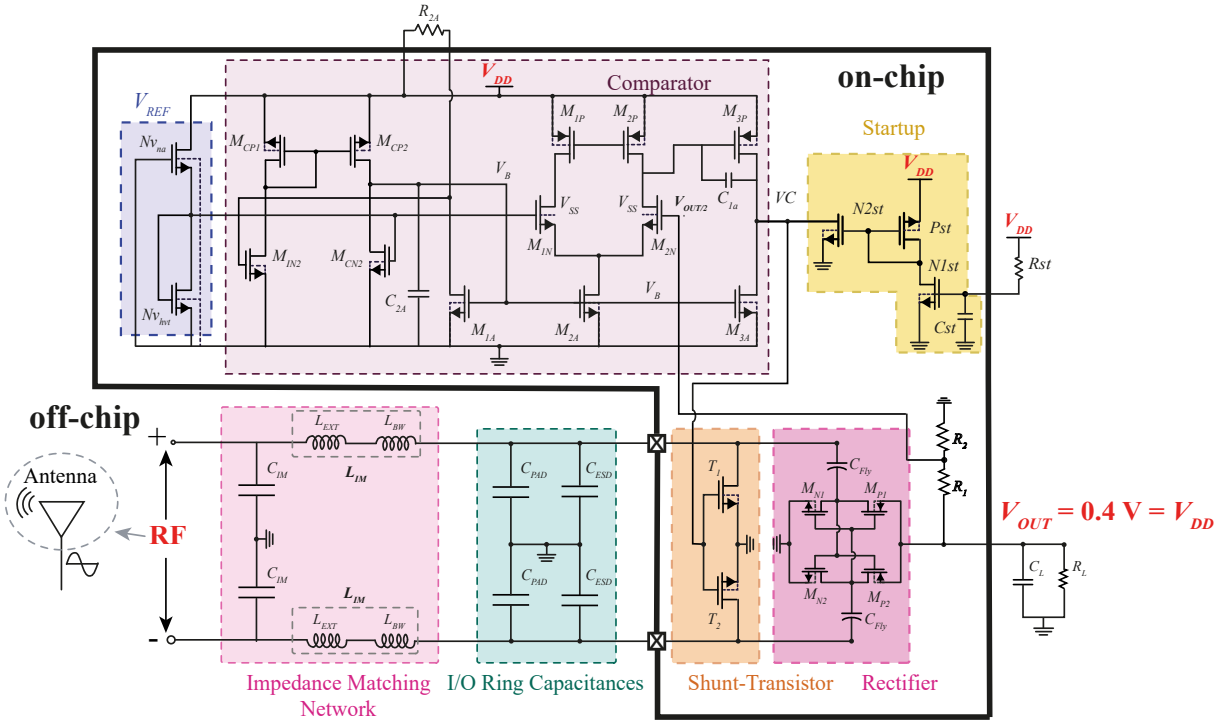
Figure 65 – Physical layout of the startup circuit.



5.4 POST-LAYOUT SIMULATION RESULTS

The complete RF-EH system in a closed loop and at the schematic level is shown in Figure 66, where some resistance and capacitance elements were considered off-chip due to their dimensions. After implementing the physical layout of each block, Figure 67 shows the system top-level, which occupies a silicon area of approximately 0.0458 mm^2.

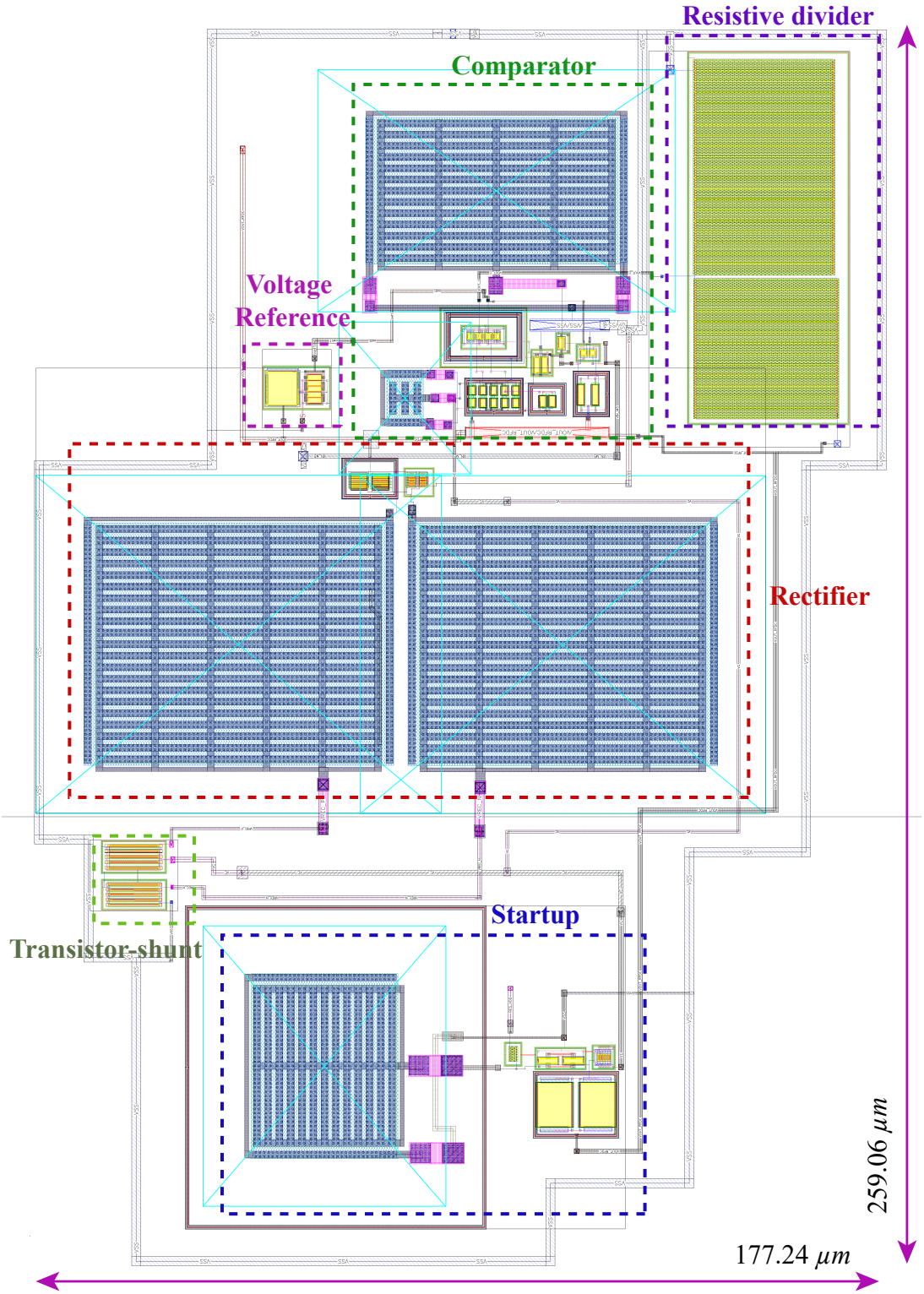
Figure 66 – Self-regulated RF-EH system at the schematic level.



To validate the regulation operation, considering the nature of the RF signal (time-varying), a post-layout transient analysis was carried out with variations of 35 mV, 70 mV, 105 mV, 140 mV, 175 mV, 210 mV, 245 mV, of the RF signal amplitude. According to Figure 68, it can be seen that compared to the open-loop system, where the system only reaches 0.4 V at maximum power transfer (V_{AMP} = 90 mV), and the closed-loop system with the shunt transistor methodology, the V_{OUT} of the RF-EH system operates over a wide range of signal amplitudes (90 mV at 245 mV).

The main parameter for validating the complete RF-EH system in this work is obtaining the ULV output voltage at a regulated 0.4 V even if the system P_{IN} increases, in order to power devices without a battery. A post-layout analysis of the output voltage as a function of the RF signal input power was therefore carried out, using Equation 5.3 and 5.4 where the value of -14.05 dBm is observed at maximum power transfer, but Figure 69a shows that the system regulates over a range of -15 dBm to -5 dBm. After obtaining the sensitivity requirement, the PCE analysis is also carried out, resulting in a peak efficiency of around 50%, as shown in Figure 69b. Both simulations have considered an emulated load of R_L = 10 kΩ.

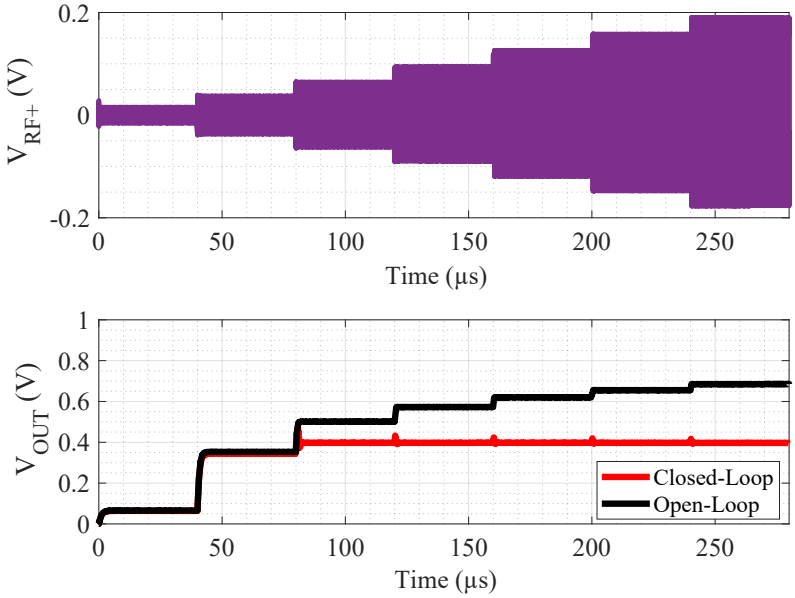
Figure 67 – Self-regulated RF-EH system at physical layout.



$$P_{IN_{(RMS)}} = RMS(V_{AMP}I_{AMP}) \tag{5.3}$$

$$P_{IN_{(dBm)}} = 10log\left(\frac{P_{IN\,(RMS)}}{1\ mW}\right) \tag{5.4}$$

Figure 68 – Post-layout analysis of the open-loop and closed-loop output voltage as a function of time for different RF signal amplitudes.

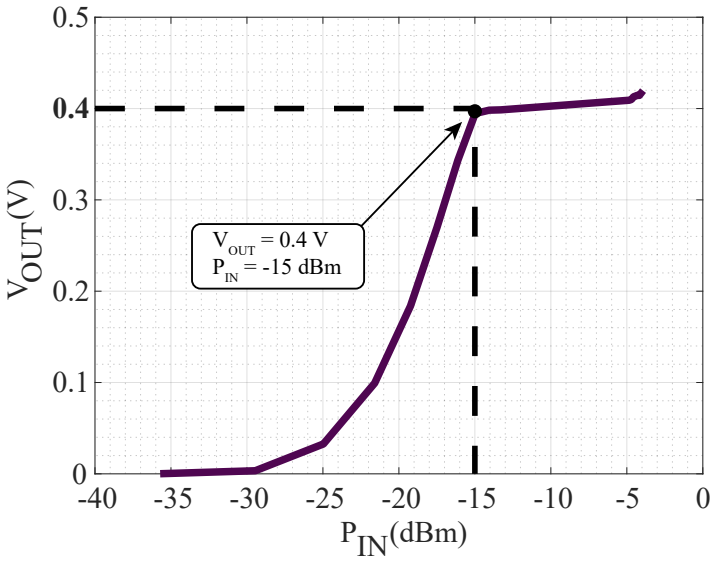


After obtaining the minimum requirements, an analysis was made of the TT (typical-typical), SS (slow-slow) and FF (fast-fast) corner models of the output voltage at the point of maximum power transfer, and as can be seen in Figure 70 where the SS model takes longer to charge, it also reaches 0.4 V. Thus, from this analysis it can be concluded that the system performs well during different variation situations.

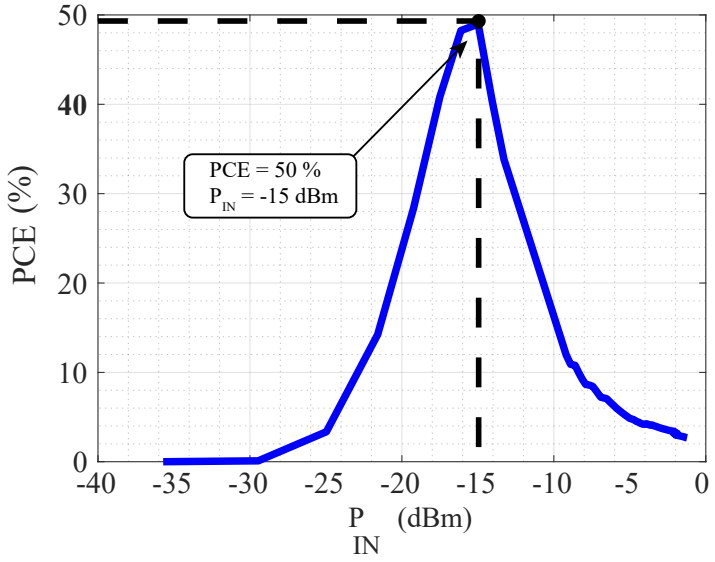
To verify the performance of the RF-EH considering different values of output load R_L, an analysis was carried out considering a dynamic variation of R_L, with fixed V_{AMP}, as illustrated in Figure 71. For this purpose, R_L was adopted with 50 kΩ, 25 kΩ, 12.5 kΩ , 6.25 kΩ, and 3.12 kΩ, where it can be seen that in the first 6 μs the system is charging, i.e. this is the moment when the start circuit should act, as soon as the start circuit is triggered, the system is started and the output voltage V_{OUT} is regulated to the desired value. This simulation also shows the behavior of the output power (P_{OUT}) of the RF-EH system, where it can be seen that for lower values of R_L, the higher the P_{OUT} obtained, as well as a wide operating range, with units of μW and tens of μW. For the ultra-low power requirements of this design, this simulation shows that the 10 kΩ load adopted satisfies the requirements.

In Table 7 a comparison was made with similar works in the literature with voltage regulation capability. It is observed that the RF-EH proposed in this work presents the best peak PCE. When compared to Yan, Kuo e Liao (2022), the RF-EH in this paper has fewer rectification stages to obtain 0.4 V, resulting in a smaller design area. However, in Yan, Kuo e Liao (2022) the output power P_{OUT} obtained is not ULP. Compared to Nagaveni et al. (2020), which uses the same CMOS process for ULP power and a similar design frequency, the RF-EH in this work also has fewer rectification stages and a better PCE result for low sensitivity. The work in Noghabaei et al. (2022) presented an RF-EH of

Figure 69 – Post-layout analysis of output voltage as a function of sensitivity and power conversion efficiency as a function of sensitivity, for $R_L = 10$ kΩ.



(a)



(b)

the same frequency, but to obtain a higher output voltage using a different CMOS process, and it is observed that for the low-voltage output, there is a need to use more rectification stages.

Figure 70 – Post-Layout analysis of output voltage corners as a function of time for the complete RF-EH system.

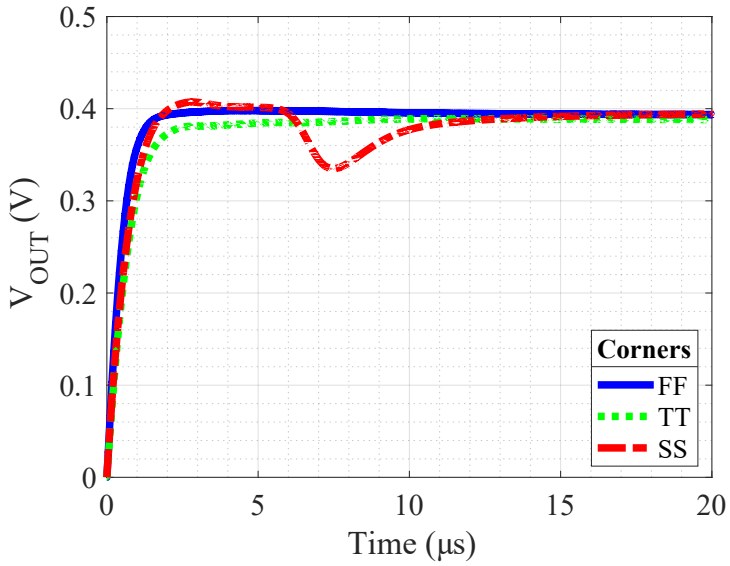
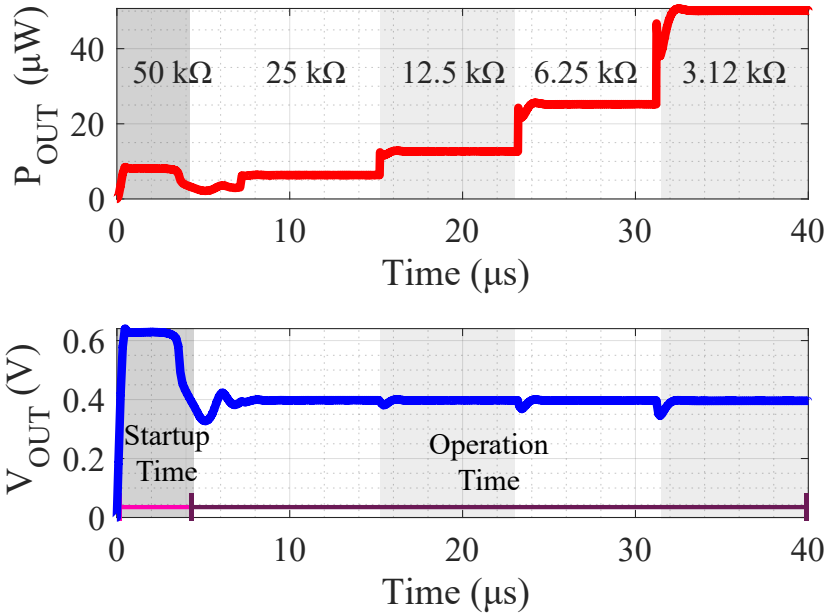


Figure 71 – Post-layout analysis of output voltage and output power for the complete closed-loop RF-EH system, with R_L variation.



5.5 IC PROTOTYPE

The full-custom MiniAsic chip RF-EH (Figure 72) using TSMC 65 nm is designed and sent for manufacture in collaboration with the Europractice service.

The complete study of this top-level chip was also carried out in this work. Having the design area available (1 mm x 1.2 mm), the number of pins that could be used was estimated, resulting in a total of 34 pins, 20 of which were intended for RF circuits. This was followed by a study in the technology PDK of the I/O PADs, ESD protections, fillers, corners and finally placement in the available area.

An I/O library from TSMC was used to implement the I/O protection ring. The

Table 7 – Performance comparison with other works from the literature.

Spec.	**This Work** $^{\triangle}$	**TCASI'22[1]***	**TCASI'20[2]***	**TCASII'17[3]**
Process (nm)	**65**	130	180	65
Freq. (MHz)	**915**	915	914/2400	900
V_{OUT} (V)	**0.4**	2.32	0.4	1
Sens. (dBm)	**-15**	-16	-16	-17.7
PCE (%)	**50**	42.8	47.1	34.5
P_{OUT} (μW)	**16**	25	32	6
N. of stages	**1**	10	3	5
Effec. area (μm^2)	**0.045**	N.A	N.A	0.048
VRC$^{\diamond}$	**Yes**	Yes	Yes	Yes

$^{\triangle}$Post-layout simulation data; *Measured data; $^{\diamond}$VRC - Voltage Regulation Capability.

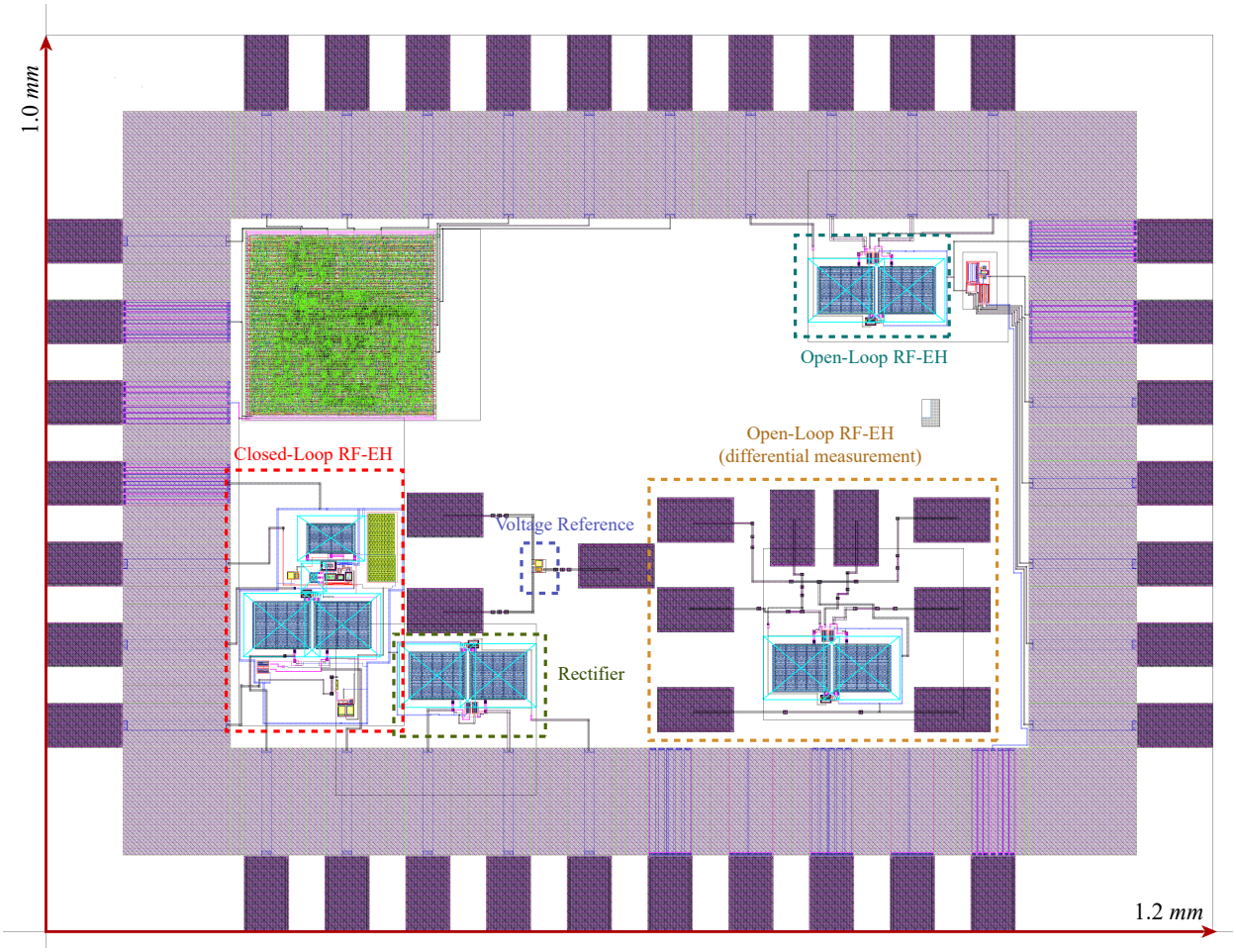
[1] - Noghabaei et al. (2022), [2] - Nagaveni et al. (2020), [3] - Yan, Kuo e Liao (2022).

implementation of analog I/O ESD of protection given by the core voltage (C_{ESD} = 326 fF) has been taken into account, in addition, for V_{DD} and V_{SS} specific ESDs are also considered for each respectively. The analog PADs are defined considering the one with the minimum capacitance, considering that the system is high-frequency (C_{PAD} = 30.10 fF) being adopted for the I/O inputs for V_{DD} and V_{SS}, with pitch of 90 μm. Four digital pins of the types are also considered as ESD for V_{SS} and V_{DD} respectively, and for the digital I/O PAD.

After placing the I/O ring on the chip, the RF circuits (closed-loop RF-EH, open-loop RF-EH, rectifier and V_{REF} with micro pads) were placed on the available die area, where there was a design area left over, which was used to implement circuits from other members of the research group. Finally, the floorplan and routing of the top-level chip (Figure 72) were made and sent for manufacture.

The test of the prototyped IC is not part of this work, although a measurement setup and a test board are detailed in Appendix A.

Figure 72 – 65-nm RF Energy Harvesting Full-chip.



5.6 CONCLUSION OF THIS CHAPTER

This chapter covered the complete design of the RF-EH system at the schematic level and layout level, presenting the detailed sizing and operation of each one of the individual blocks. Simulations of the RF-EH in the closed loop with self-bias at the post-layout level were carried out, showing that the system reaches a peak PCE of 50% for a sensitivity of -15 dBm for an output voltage of 0.4 V, as initially specified in this work. Voltage regulation over a wide voltage range of the RF signal amplitude, corner analysis and a load analysis were also shown, demonstrating the high performance of the developed system. Finally, this work showed the prototyping of the 65 nm chip, as well as details about placement, floorplanning and routing of the RF-EH system and the most important RF circuits for its electrical validation.

6 CONCLUSION

This dissertation presented the development of a complete RF-EH system that is capable of harvesting RF energy from the environment at a frequency of 915 MHz and converting it into an ultra-low voltage of 0.4 V to serve as a power source for electronic devices operating at ultra-low-power. It is suitable for devices located in hard-to-reach places, such as biomedical implants, with the capacity of replacing the use of batteries in these devices.

To do this, we first studied the principle of wireless communication and RF Energy Harvesting, considering the main and most recent approaches in the literature, in order to develop a system that is innovative, efficient and sensitive to collect RF signals with low power levels.

In addition, a study was also carried out on different forms of voltage regulation, in order to make the RF-EH system provide an output voltage of 0.4 V for the end devices in a high input power range. The system was implemented in three versions in this work, concluding that the voltage regulation version using shunt transistors is the most efficient and has the greater regulation range.

The RF-EH was implemented at schematic and layout levels using a CMOS 65-nm process, in which all the designed parts were described in detail. The results showed that an integrated closed-loop self-sustained regulation system is obtained. It is able to regulate the output voltage for a range of amplitude values of the input RF signal and for a range of output load values, presenting a sensitivity of -15 dBm with a peak PCE of 50%. In addition, the design also demonstrates the use of only one rectification stage to obtain ultra-low output voltage, using the CCDD rectifier, which makes the design simpler.

The RF-EH system designed in this work showed post-layout results, considering variations in corners, variations in RF signal amplitude, and also variations in load resistance. The system starts automatically with 90 mV of V_{AMP} in 7 μs, using a startup which allows self-biasing of the control circuits. It keeps the output voltage regulated after the startup time. When compared to other works in the literature that have voltage regulation ability, the proposed circuit presented satisfactory and competitive performance. The complete layout of the RF-EH system resulted in an effective silicon area of 0.045 μm^2.

A complete IC was designed and sent to fabrication to validate the RF-EH system proposed in this work. Unfortunately, due to the long time expended in the fabrication and delivery process to Brazil, it was not possible to perform the measurements before the end of this work.

As contributions, during the development of this work some papers have been published in conferences and journals:

- DE-OLIVEIRA, Tailize C. et al. An RF-EH Employing Controlled-Impedance Matching for Ultra-Low Voltage Batteryless Devices. In: 2023 IEEE 14th Latin

America Symposium on Circuits and Systems (LASCAS). IEEE, 2023. p. 1-4.

- DE-OLIVEIRA, Tailize C. et al. A 915-MHz RF-EH with Varactor-Based Adaptive Impedance Matching for ULV Batteryless Devices. In: 2023 Argentine Conference on Electronics (CAE). IEEE, 2023. p. 112-116.

- DE-OLIVEIRA, Tailize et al. A 915 MHz Closed-Loop Self-Regulated RF Energy Harvesting System for Batteryless Devices. Journal of Integrated Circuits and Systems, v. 18, n. 3, p. 1-11, 2023.

- DE-OLIVEIRA, Tailize C. et al. A 5.8-GHz RF VCO-Based Sensing System with Integrated RF Energy Harvesting in CMOS 65-nm for Health Monitoring Applications. In: 2024 IEEE 15th Latin America Symposium on Circuits and Systems (LASCAS). IEEE, 2024.

As a researcher during this academic master period, the author also contributed to the development of the following papers in correlated areas:

- GIRARDI, Alessandro et al. A Comprehensive Review on Automation-based Sizing Techniques for Analog IC Design. Journal of Integrated Circuits and Systems, v. 17, n. 3, p. 1-14, 2022.

- SANTOS, Suzian Mahéli R. et al. A Negative Resistance-Based ULV Variable-Gain OTA for Low-Power Applications. IEEE Transactions on Circuits and Systems, II: Express Briefs, 2023.

- COMPASSI-SEVERO, Lucas et al. Variable Conversion Approach for Design Optimization of Low-Voltage Low-Pass Filters. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2023.

- DE OLIVEIRA, Raul P. et al. A 915 MHz Active Inductor-Based Band-pass Filter for sub-GHz RF Receivers. In: 2023 Microelectronics Students Forum. SBMicro, 2023.

- DE OLVIERA, Raul P. et al. A CMOS 65nm UHF BandPass Filter Employing Active Inductor for Small-Satellites. In: XLI Simpósio Brasileiro de Telecomunicações e Processamento de Sinais. 2023.

Finally, we propose the following activities as future work for the continuation of research on this topic:

- The experimental validation of the designed RF-EH IC, following the test guide available in Appendix A;

- The study of novel techniques to design the RF-EH system for higher frequencies, such as 2.5 GHz and 5.8 GHz, or make the RF-EH compatible with more than one signal band;
- The study and improvement of the start-up circuit to make it smarter
- The study of RF-DC circuits combined with integrated DC-DC converters to generate different output voltage levels;
- The development of new design methodologies taking into account the parasitic effects of the layout during the early stages of the circuit.

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APPENDIX A – IC MEASUREMENT TEST PLAN

The IC developed in this work is designed for RF Energy Harvesting and must convert the input power of a 915-MHz RF signal into a DC voltage of 0.4 V with a sensitivity of -15 dBm and a PCE of 50%, at maximum power transfer. Thus, when there are variations in the amplitude of the input RF signal, or variations in the output load, the RF-EH system must be able to regulate and maintain the desired output voltage. Therefore, to ensure that the results measured with the Cadence Virtuoso tool are true, and to prove the RF-EH methodology presented in this work, the chip was prototyped and a measurement plan will be presented below.

The circuits that will be measured for scientific proof in the prototyped IC are the RF-EH open-loop and closed-loop, the rectifier (as it is the main block that converts frequency to DC) and the voltage reference (which provides the voltage to be compared in order to perform voltage regulation), so the first step is to plan these measurements.

To do this, as illustrated in Figure 72, the closed-loop RF-EH, the open-loop RF-EH and the rectifier will be measured externally by connecting to a 915-MHz antenna and the voltage reference will be measured using microdots and a second the open-loop RF-EH will be measured using differential microdots.

For the measurement using the PADs, a printed circuit board (PCB) will be presented to insert the chip and the impedance matching (defined in the course of the work as off-chip). To do this, as shown in Figure 73 a testbench schematic was developed using the EasyEda online tool, which contains the chip developed, the IMN, the output RC load and the resistors contained in the voltage regulation circuit which (external).

For the open and closed loop RF-EH circuits, an impedance match was considered containing a PI network with LC elements and two inductors in series. The PI network is used as an option in case changes need to be made during the measurement, and the two inductors in series are used to obtain the inductance of approximately 70 nH that the circuit needs to be matched.

To enable RF input from a 915-MHz antenna with 50 Ω, SMA connectors of the HX SMA P 9501 type were used. For the differential inputs of the RF circuits, a TCM1-63AX+ balun was used to collect the 915-MHz signal. Thus, the RF input can be single-ended and connected to the 915 MHz receiving antenna.

For the schematic PCB design, we also considered the microstrip method to calculate the transmission line (TL) that will be used to connect the RF signal input to the chip. To do this, the width of the TL was calculated using the TXLine software by Cadence Design Systems. As shown in Figure 74, we have considered the Rogers corporation RO4003C laminate and its electrical characteristics are considered in this calculation, obtaining a TL width of 1.78 mm.

Variable resistors (trimpots) are used to measure the output voltage, so that it is possible to adjust the resistors externally, i.e. to replicate the simulation seen in Figure 71

Figure 73 – PCB schematic for chip testing.

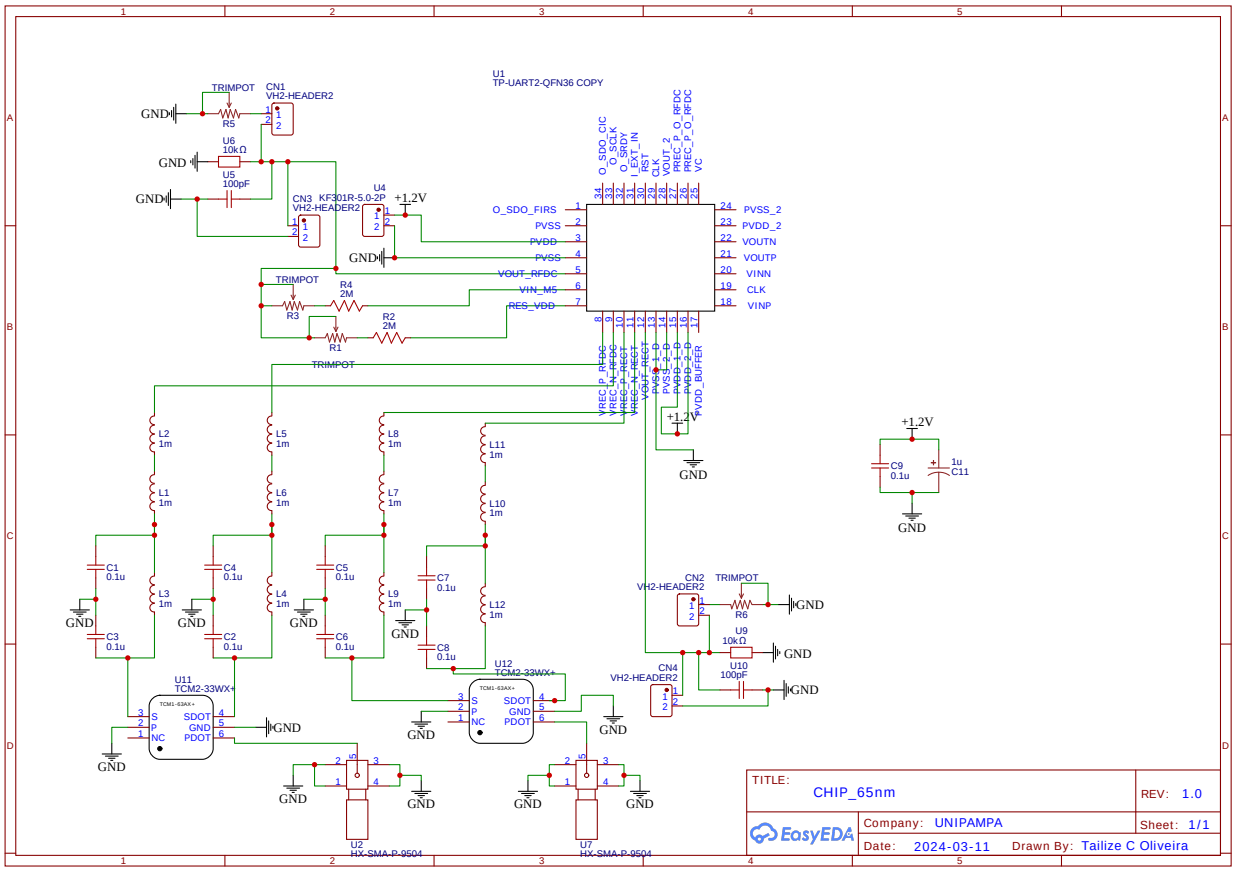
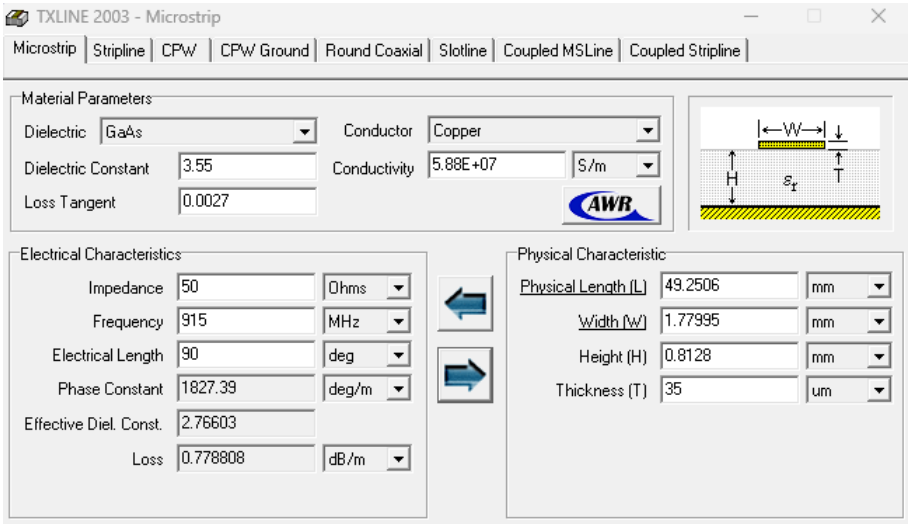


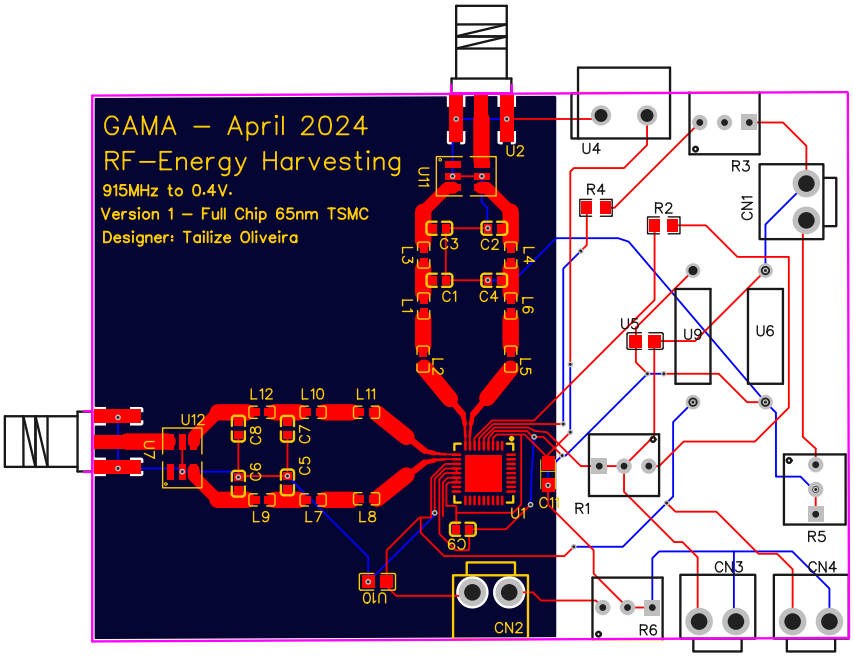
Figure 74 – LT thickness calculation using TXline software.



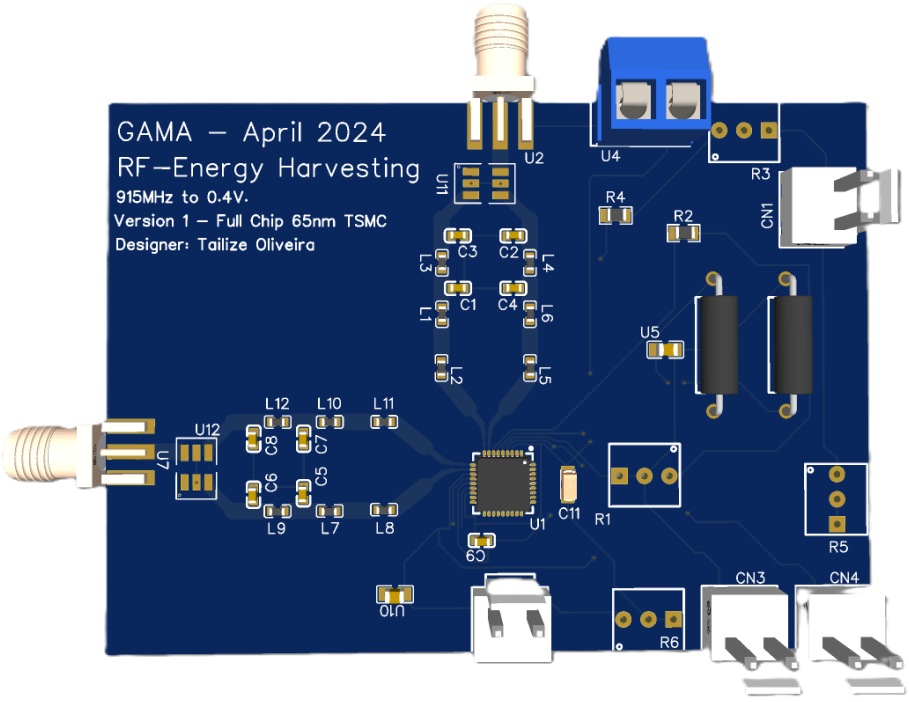
where, for different resistors, the RF-EH system's voltage must be regulated. In addition, trimpots are also used to adjust the resistors contained in the startup and comparator externally. Pins of type CN1 VH2-HEADER2 are adopted on all outputs for voltage and current measurement.

After making the PCB schematic, the connection layout for all the proposed components is shown in Figure 75 with dimensions X = 79.3 mm and Y = 59.3 mm,

Figure 75 – PCB layout for chip testing. a) 2D layout; b) 3D layout.



(a)

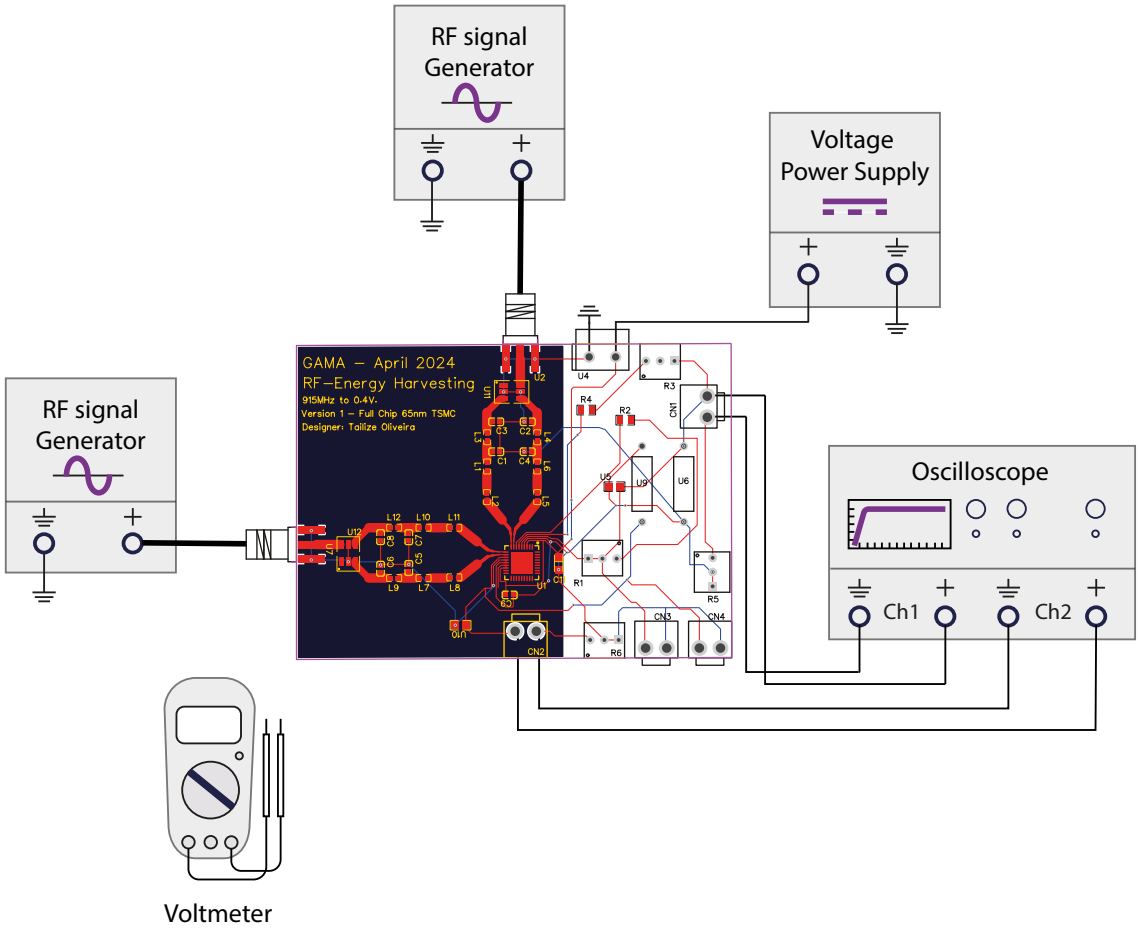


(b)

which will be developed in the GAMA laboratory at the Federal University of Pampa. In addition, another PCB will be developed just for LT characterization testing and equipment calibration.

The suggested measuring equipment is illustrated in Figure 76 and includes the proposed printed circuit board, an RF signal generator (to generate the design frequency), a voltmeter to measure the output voltage, an oscilloscope to plot and observe the output

Figure 76 – IC Measurement test plan.



voltage as a function of time. In addition, the V_{DD} voltage will also be tested using a DC voltmeter.